EXHIBIT A

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY
Patent Owner

IPR2022-00252
U.S. Patent No. 7,498,633

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 7,498,633
CHALLENGING CLAIMS 9–11
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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STMicroelectronics, Inc. ("Petitioner") respectfully requests *inter partes* review ("IPR") of claims 9–11 of U.S. Patent No. 7,498,633 (the "'633 patent") (EX1001) pursuant to 35 U.S.C. §§ 311–19 and 37 C.F.R. § 42.1 *et seq.*

I. INTRODUCTION

The '633 patent is directed to semiconductor devices, such as metal-oxide semiconductor field-effect transistors (MOSFETs), for high-voltage power applications. The problem described by the '633 patent and its alleged solution, however, were well-known in the art, as detailed in the ground below.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner STMicroelectronics, Inc. ("ST") is a real party-in-interest. Although STMicroelectronics N.V., ST's parent company, and STMicroelectronics International N.V., which is under common ownership with ST, are not real parties-in-interest under the governing legal standard for making that determination, ST identifies them as real parties-in-interest for purposes of this Petition to avoid any disputes over that issue.

B. Related Matters

According to USPTO records, the '633 patent is owned by The Trustees of Purdue University ("Patent Owner" or "PO"). Petitioner knows of the following co-pending litigations involving the '633 patent: *The Trustees of Purdue University v.*

STMicroelectronics N.V. and STMicroelectronics, Inc., No. 6:21-CV-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). The earliest date of service on Petitioner in the co-pending litigation was July 20, 2021.

C. Counsel

Under 37 C.F.R. §§ 42.8(b)(3)–(4), Petitioner identifies the following lead and backup counsel, to whom all correspondence should be directed.

Lead Counsel:	Richard Goldenberg (Reg. No. 38,895)
Backup Counsel:	Gregory Lantier (*pro hac vice* to be filed)
	Scott Bertulli (Reg. No. 75,886)
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Petitioner consents to service by e-mail on lead and backup counsel.

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") at the time of the earliest claimed priority date[1] of the '633 patent would have had the equivalent of a Bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa. EX1002, ¶23.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the patent for which review is sought is available for IPR and under 37 C.F.R. §§ 42.101(a)–(c) that Petitioner is not barred or estopped from requesting an IPR challenging the patent claims on the ground identified in this Petition.

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[1] PO contends in the co-pending litigation that the earliest date of invention for claim 9 of the '633 patent is April 26, 2004. EX1025. Petitioner does not concede—and does not believe—that any of the challenged claims are entitled to benefit of that date ***or*** the filing date of U.S. Provisional Application No. 60/646,152. Regardless, the references relied upon herein are prior art.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Claims for Which Review is Requested and Ground on Which the Challenge is Based

Under 37 C.F.R. §§ 42.22(a)(1) and 42.104(b)(1)–(2), Petitioner requests cancellation of claims 9–11 of the '633 patent on the following ground:

Ground	References	Basis	Claims Challenged
I	*Ryu* in view of *Williams*	§ 103	9–11

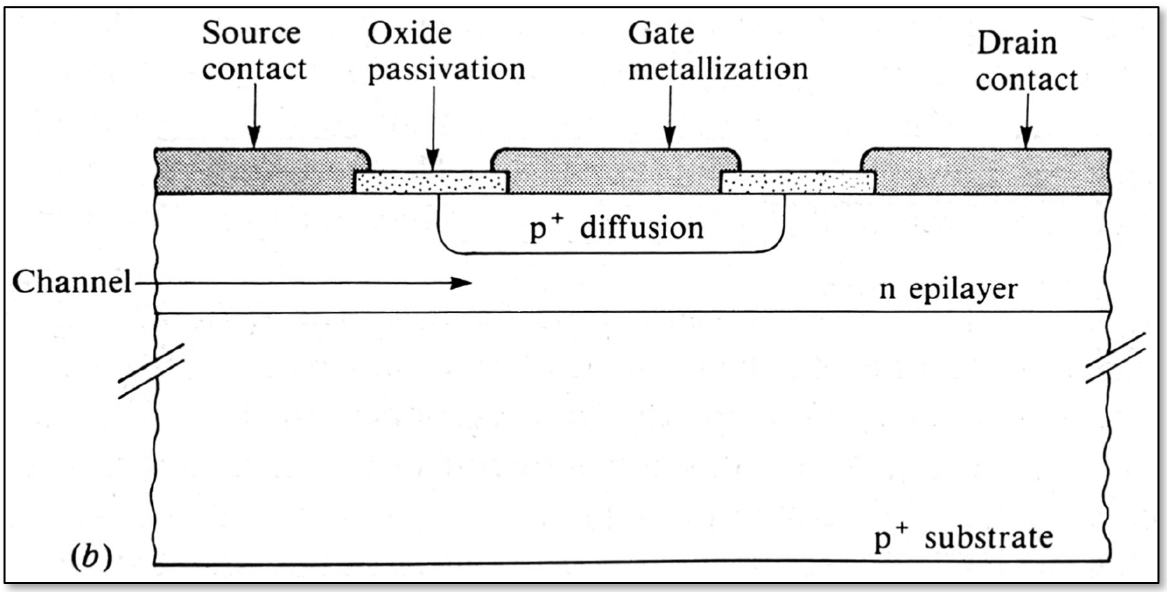
This Petition, supported by the declaration of Dr. Subramanian (EX1002), demonstrates that there is a reasonable likelihood Petitioner will prevail with respect to cancellation of at least one of the challenged claims. *See* 35 U.S.C. § 314(a).

VI. TECHNOLOGY BACKGROUND

A. Field-Effect Transistor ("FET")

A field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor. *See* "Power MOSFETs – Theory and Applications," Duncan A. Grant and John Gowar, 1989 ("*Grant*"), EX1019, 1 ("The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most commonly used active device in the very large-scale integration of digital integrated circuits …. The conductance of a piece of semiconductor depends on the number of free carriers it contains and on their mobility. The effective number of free carriers can be modified by establishing a static electric field in the

semiconductor in the direction transverse to the current flow."). A FET generally includes a source, a drain, and a gate, as *Grant* illustrates in a cross section of a junction field-effect transistor (JFET) in Figure 1.1, reproduced below. *See, e.g.*, *id.*, 2. The flow of current is controlled by applying a voltage (*i.e.*, creating an electric field) to the gate, altering the conductivity of the channel formed between the drain and the source. *See id.*, 3. EX1002, ¶¶24-25.

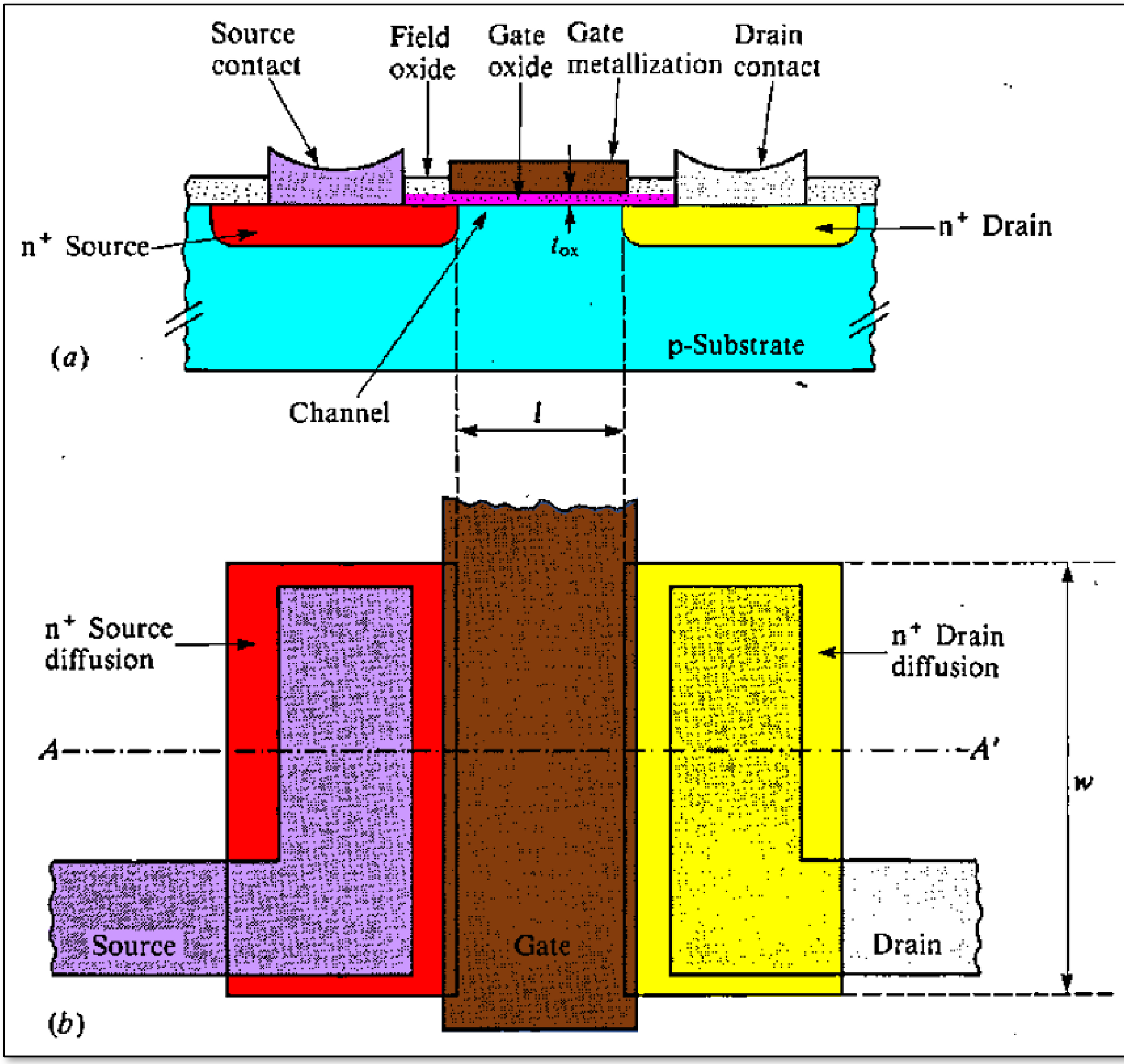


EX1019, Figure 1.1

Grant notes that "[t]he successful manufacture of the JFET depended on the introduction of *planar* silicon technology in 1960" that involves a "combination of processes," including epitaxial crystal growth, photolithographic etching of windows in the oxide layer, and introduction of controlled levels of impurity (*i.e.*,

doping) into selected regions of the silicon by diffusion or implantation. EX1019, 3. EX1002, ¶26.

"Further technological refinements in the early 1960s enabled a different type of field-effect transistor to be made. This was the metal-oxide-semiconductor field-effect transistor (MOSFET)." EX1019, 5. *Grant* points out that the difference between a JFET and a MOSFET is "[t]he controlling gate electrode is now separated from the semiconductor by a thin insulating layer of gate oxide, as shown in Figure 1.3." *Id.*; *see also* U.S. Patent No. 5,233,215 ("*Baliga*") (EX1005), 1:45–50.. In Figure 1.3 (reproduced below), *Grant* illustrates a cross section and a plan view of a MOSFET. EX1019, 5. When the MOSFET is turned on, current can flow between the source and drain through the channel, shown in the figure and formed in the p-type substrate. The source region is annotated in red, drain region in yellow, p-type substrate in cyan, gate in brown, gate oxide in magenta, and source contact in lavender. The source contact is often referred to as "source metallization," "source metal," or "source electrode." *See* EX1019, Figure 1.13 (illustrating the source metallization); EX1015, Figure 1, 1:38 ("source metal"); EX1005, 2:64 ("source electrode"). EX1002, ¶27.



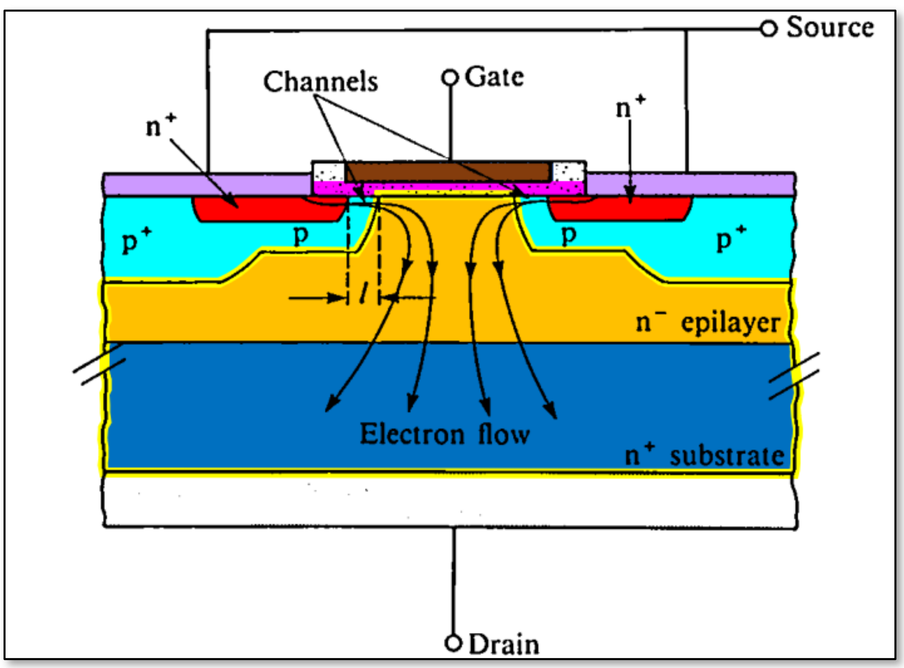
EX1019, Figure 1.3 (annotated)

B. Power MOSFET

The MOSFET became "important in devices designed for power applications." EX1019, 5; *see also* EX1005, 2:14–16 ("many variations of power MOSFETs have been designed for power devices."). *Grant* notes that "the decision as to what constitutes a power device is quite arbitrary" and the term is applied to

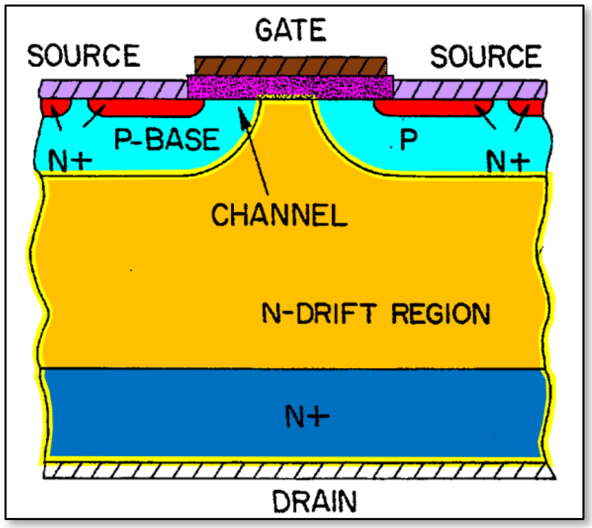
"any device capable of switching at least 1 A" (*i.e.*, turning on and off a current of 1 ampere flowing from the drain to the source). EX1019, 5–6. EX1002, ¶28.

Grant further notes that "the planar structure of Figure 1.3 is unsatisfactory if it is simply scaled up for higher powers." EX1019, 8. One solution well known in the art was to change the lateral structure as illustrated in *Grant*'s Figure 1.3 to a vertical structure that uses the substrate material to form the drain region such that "the current flows 'vertically' through the silicon from drain to source." *Id.* This change led to the ***vertical double-diffused MOSFET***, which *Grant* illustrates in Figure 1.11, reproduced below. *Id.*, 13–14. EX1002, ¶29.



EX1019, Figure 1.11 (annotated)

Baliga also illustrates a vertical double-diffused MOSFET in Figure 1, which is reproduced below. EX1005, 6:12–13 ("FIG. 1 is a cross-sectional view of a known DMOSFET device"). EX1002, ¶30.



EX1005, FIG. 1 (annotated)

The term "double-diffused" derives from a manufacturing technique commonly used to form the n+ source regions within the p-type body region: "[t]he p-type 'body' region . . . and the n+ source contact regions are diffused successively through the same window etched in the oxide layer." EX1019, 14; *see also* EX1005, 2:35–38. The p-type body region is often referred to as "p-type wells" or "p-base regions." *See, e.g.*, EX1019, 146 ("p-type wells"); EX1005, 2:35 ("p-base region"), Figure 1 (illustrating p-base regions). EX1002, ¶31.

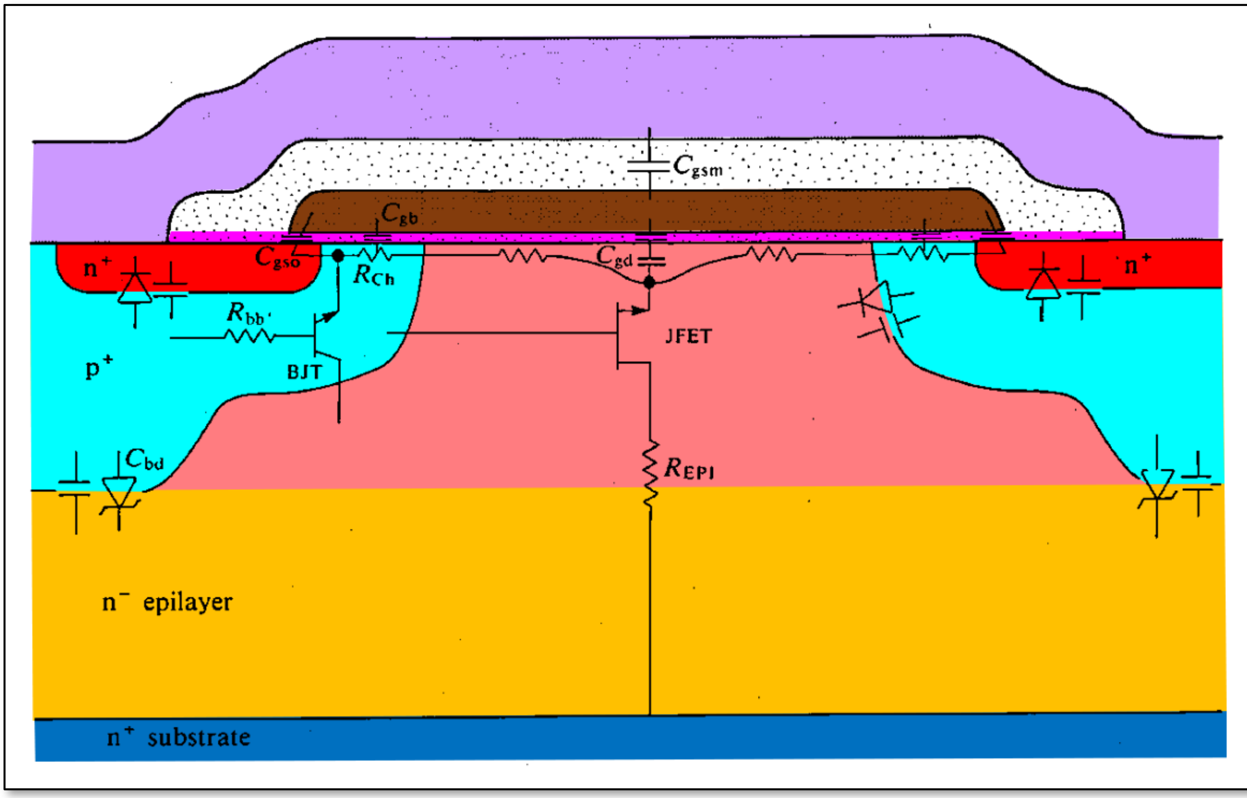
In each of the above *Grant*'s Figure 1.11 and *Baliga*'s Figure 1, the source regions are annotated in red, p-type body regions in cyan, gate in brown, gate oxide

in magenta, and source contacts in lavender. The drain region (outlined in yellow) comprises the substrate (annotated in blue) and the epilayer (annotated in orange). Electrons flow from the source to the drain through the channels formed in the p-type wells, the epilayer, and the substrate. The epilayer is often referred to as the "drift region." *Grant* notes that "[t]he drain drift region is particularly critical to the design of a power MOSFET" because "[i]ts principal function is to block and support the full forward voltage held off by the transistor in its turned-OFF state" and "it has also to carry the full forward current in the ON state." EX1019, 74. EX1002, ¶32.

C. On-Resistance

According to *Grant*, "[t]he minimization of the ON-state voltage drop is an important consideration in power devices." EX1019, 18. This ON-state voltage drop depends on the "ON-state drain-source resistance, $R_{DS(on)}$"—also known simply as the "on-resistance." *Id.* U.S. Patent No. 6,413,822 to Williams and Grabowski ("*Williams*") explains that the on-resistance of a MOSFET is determined by the "sum of its resistive components." EX1004, 1:33–37. *Williams* notes that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." *Id.*, 1:50–52. EX1002, ¶¶33-34.

Grant describes that the vertical MOSFET structure includes parasitic elements at junctions of n-type and p-type regions. EX1019, 79-81. In particular, *Grant* describes the existence of a parasitic "n-channel junction field-effect transistor (JFET) that forms in the epilayer, in between the channel diffusions." *Id.*, 81. *Grant* illustrates this parasitic JFET in Figure 3.15, reproduced below. *Id.*, 80, Figure 3.15. *Grant* explains that "[t]he JFET action occurs in the region between the p diffusions." *Id.*, 81. Accordingly, this region is typically referred to as the "JFET region." *See, e.g.*, EX1003, ¶44. The JFET region is annotated in pink in *Grant*'s Figure 3.15 below. *Grant* points out that "[i]ncreasing the donor doping concentration in the drain throats [(*i.e.*, the JFET regions)] . . . has two beneficial effects"—"the cell size can be reduced and . . . lower $R_{DS(on)}$ can be realized." EX1019, 83–84. EX1002, ¶35.



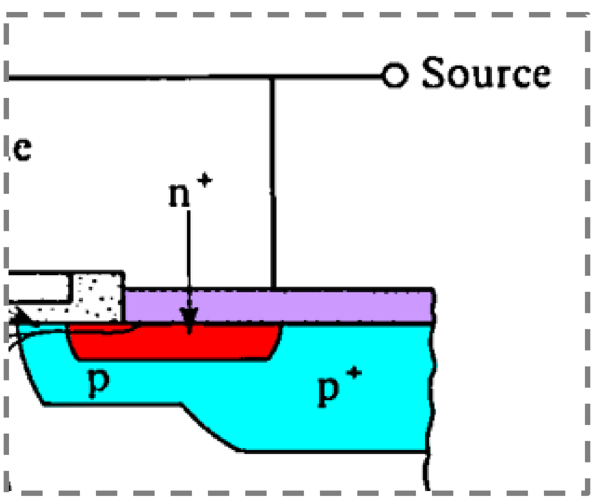
EX1019, Figure 3.15 (annotated)

Also to reduce the on-resistance, *Williams* discloses topological configurations (the physical shape, size, and arrangement of the structures) that minimize the source contact resistance, as will be discussed in more detail below. *See* EX1004, 10:17–18; 16:28–35. EX1002, ¶36.

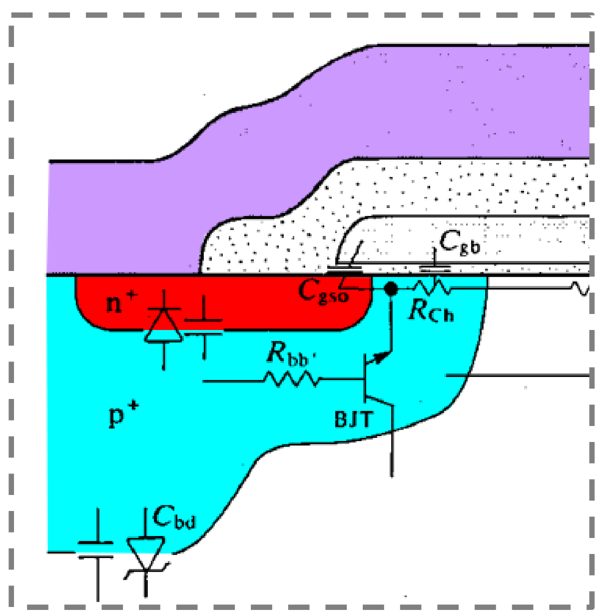
D. Unwanted Activation of Parasitic Components—Latch Up

Grant notes, and illustrates in Figure 3.15, an "npn bipolar junction transistor (BJT) formed between the source, the body, and the drain." EX1019, 81. The parasitic BJT "may be activated, and this can seriously degrade the overall performance of the MOSFET." *Id.*; *see also* EX1007, ¶¶ 6–7. Preventing unwanted

activation of parasitic components is a standard design consideration in integrated circuit design and in some contexts unwanted activation of parasitic components is known as "latch up." To prevent unwanted turn on, "[t]his parasitic bipolar transistor must be kept inactive during all modes of operation of the power MOSFET." EX1016, 266. "To accomplish this, the P-base region is short-circuited to the N^+-emitter region by the source metallization . . ." *Id.*; *see also* EX1004, 6:8–14. Indeed, as depicted by the annotated excerpts below, it was well known to electrically connect (*i.e.*, short) the p-type body or p-base region (*i.e.*, the base of the parasitic BJT; annotated in cyan) to the source region (*i.e.*, the emitter of the parasitic BJT; annotated in red) by an overlying and contacting source metallization (annotated in lavender) to keep the parasitic BJT inactive. *See, e.g.*, EX1019, 2, 80 (Figures 1.11 and 3.15); EX1005, Figure 1. EX1002, ¶37.

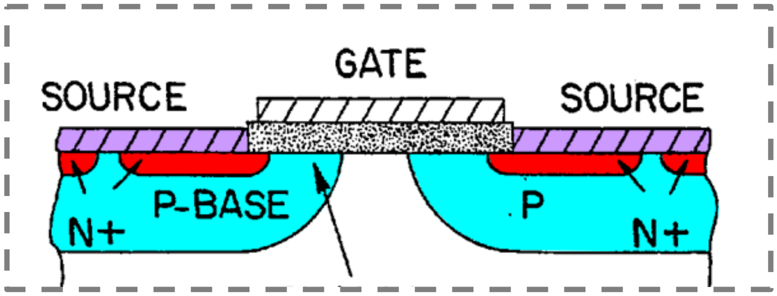


EX1019, Figure 1.11



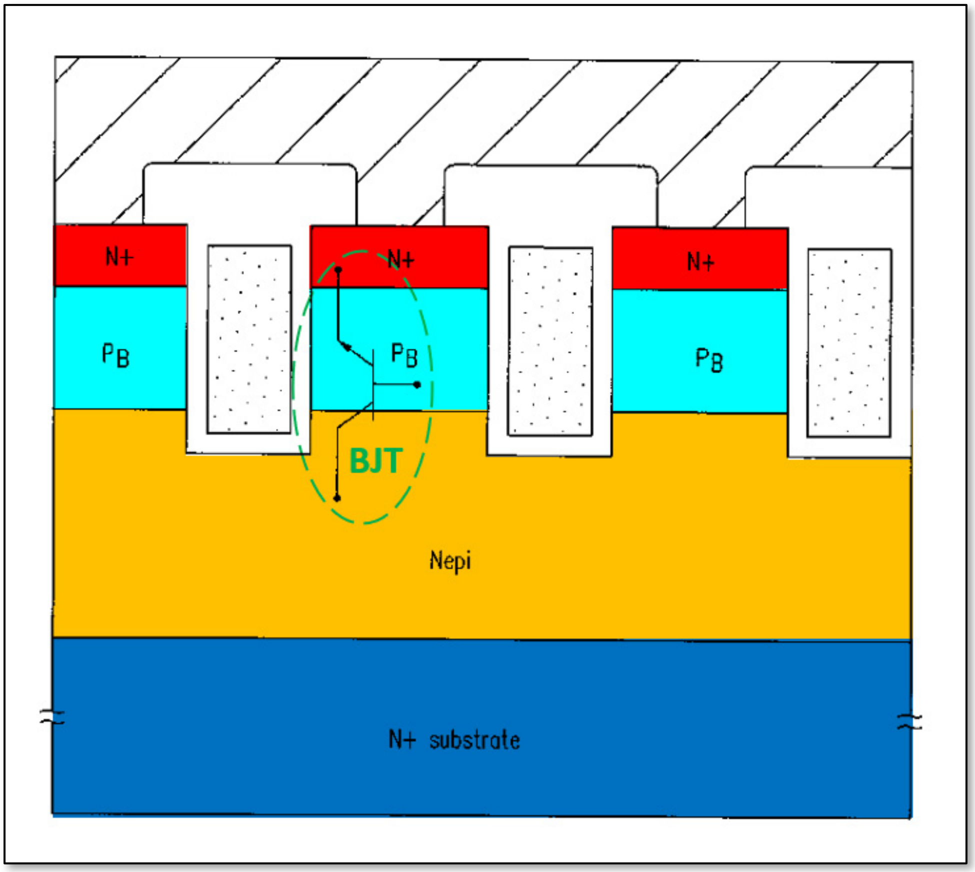
EX1019, Figure 3.15

(excerpted and annotated)	(excerpted and annotated)



EX1005, FIG. 1(excerpted and annotated)

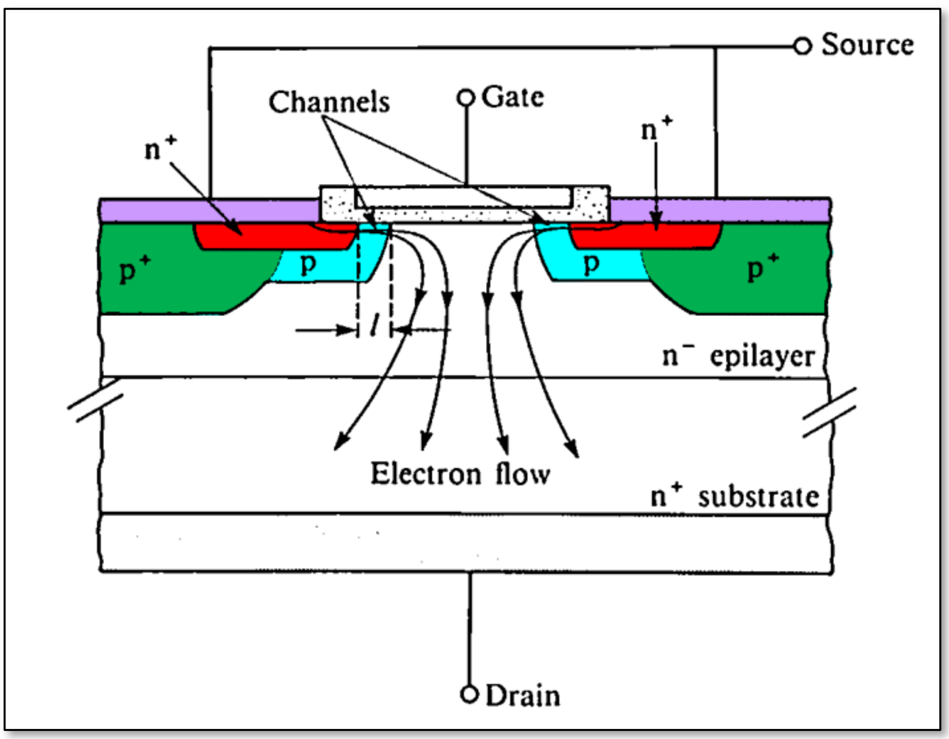
Such a parasitic BJT exists in any power MOSFET, regardless of the gate configuration, because the source, body, and drain form an npn configuration, *i.e.*, two regions of n-type semiconductor material separated by p-type material. For instance, *Williams* describes and illustrates in Figure 7A (reproduced below) a "parasitic NPN bipolar transistor" in a trench-gate vertical MOSFET. EX1004, 6:9. EX1002, ¶38.



EX1004, FIG. 7A (annotated)

Grant further explains that current flowing through the resistance $R_{bb'}$ (*see Grant*'s Figure 3.15, reproduced above) at the base of the parasitic BJT causes an ohmic voltage drop which, if it exceeds about 0.6 V, "will initiate transistor action in the parasitic BJT." EX1019, 87. To reduce resistance and minimize voltage drop, *Grant* notes that "[t]he use of the p+ diffusion to connect the body region back to the source contact can be seen to be an important part of the VDMOS FET design." *Id.*, 90; *see also id.*, 2, 16 (Figures 1.11 and 1.13(a)) (illustrating p+ diffusion in p-type body regions). "It reduces $R_{bb'}$ . . ." *Id.*, 90. Thus, in addition to connecting the

body region to the source region, a MOSFET may be ruggedized against inadvertent activation of the parasitic BJT by having p+ diffusion in the p-type body region to reduce the resistance $R_{bb'}$ and keep the ohmic voltage drop low. *See also* EX1004, 16:32–34 ("maximize the P+ contact to the body region (to suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device)"); EX1021, 5:28–30 ("Although an electrical connection can be made directly to the p type base region, the p+ base contact region provides an improved connection."). The p+ diffusions of *Grant*'s Figure 1.11 below are annotated in green. EX1002, ¶39.



EX1019, Figure 1.11 (annotated)

E. Silicon Carbide (SiC)

Historically, power MOSFETs were fabricated using silicon. But by the early 1990s, an alternative material—silicon carbide (SiC)—was also known to be particularly well suited for use in such devices. EX1005, 4:22–27 ("Almost all power MOSFETs being marketed today are fabricated in monocrystalline silicon . . . [,] as is known to those skilled in the art, crystalline ***silicon carbide is particularly well suited*** for use in semiconductor devices, and in particular, for power semiconductor devices.").[2] SiC was known to have many benefits. *Id.*, 4:27–31. "These characteristics would allow silicon carbide power devices to operate at higher temperatures, higher power levels and with lower specific on resistance than conventional silicon based power devices." *Id.*, 4:31–34; *see also* U.S. Patent No. 5,510,281 ("*Ghezzo*") (EX1021), 1:52–56. EX1002, ¶40.

Moreover, *Baliga* teaches that "power MOSFET such as the above described DMOSFET . . . can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:35–38. *Baliga* explains how to translate the DMOSFET into a SiC device using known manufacturing techniques, *e.g.*, by using higher temperature, and longer, diffusions to compensate for the lower diffusion coefficient in SiC. *Id.*, 4:38–43. *Ghezzo*, which was filed in 1995, further teaches

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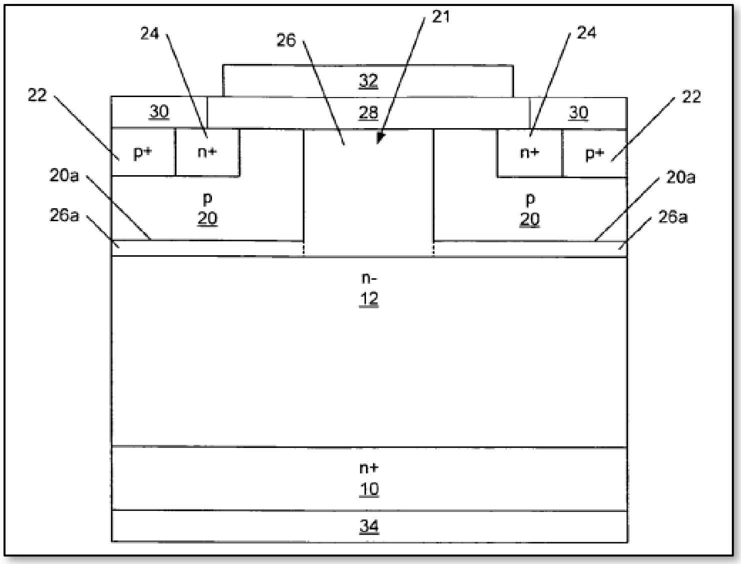
[2] Unless otherwise noted, all emphasis has been added.

that "[a] method of implementing vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted ***double ion implantation*** sequence to overcome the problem of very small dopant diffusivity in SiC" and that "[t]he channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base and source regions, respectively." EX1021, 1:56–63. SiC power MOSFETs are sometimes referred to as "double-implanted" MOSFETs to distinguish the fabrication technique used to make them from "double-diffused" used in silicon. EX1002, ¶41.

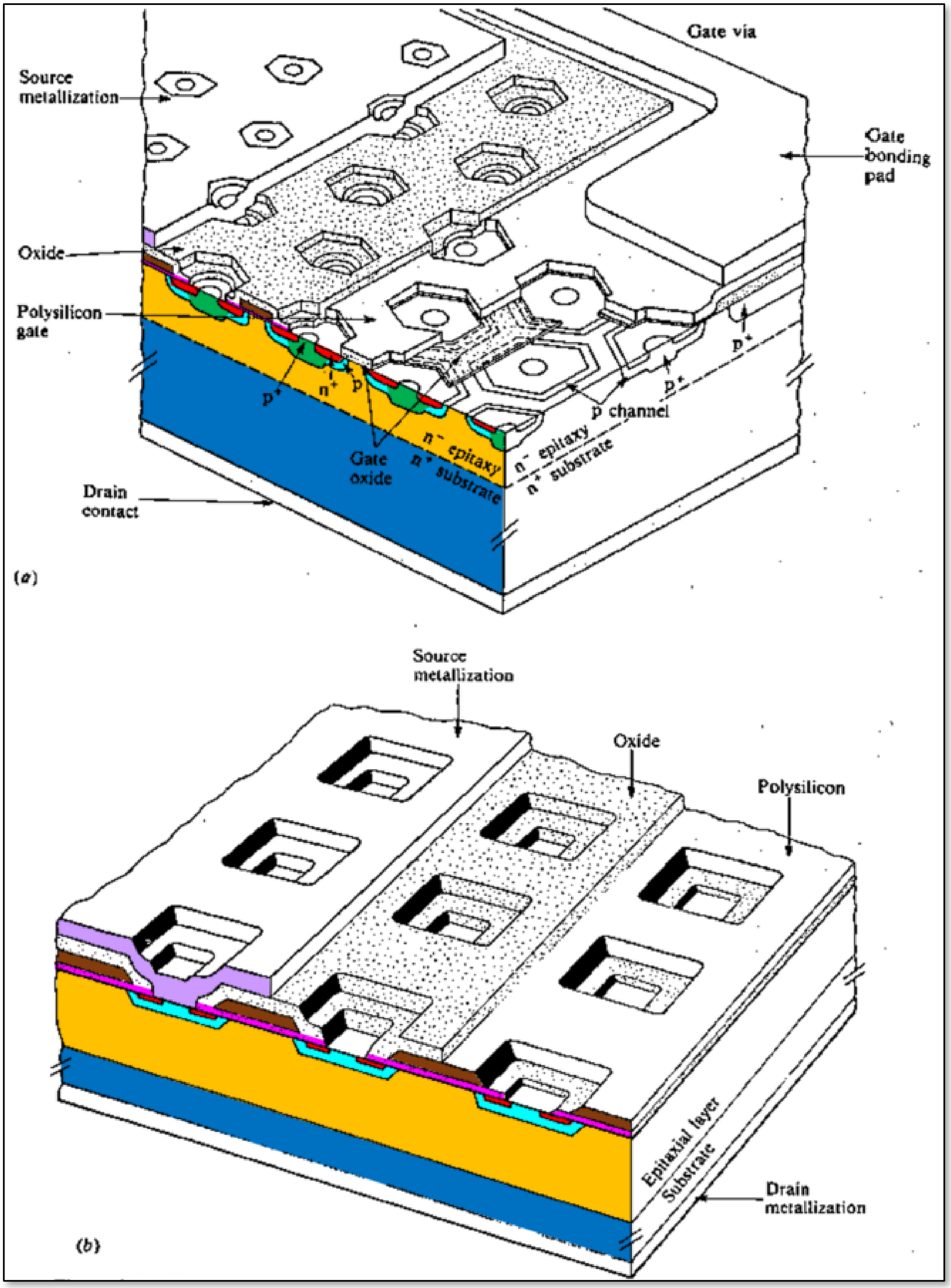
F. Visualizing Three-Dimensional Semiconductor Structures

Prior art references conventionally use a two-dimensional cross-sectional view to depict a unit cell of a power MOSFET (*e.g.*, as in *Grant*'s Figure 1.11 and *Baliga*'s Figure 1, both reproduced above). U.S. Patent Application Publication No. 2004/0119076 to Ryu ("*Ryu*") (EX1003) shows a similar example of a cross-sectional view of a unit cell of a MOSFET in Figure 2A. *See* EX1003, ¶51. EX1002, ¶42.



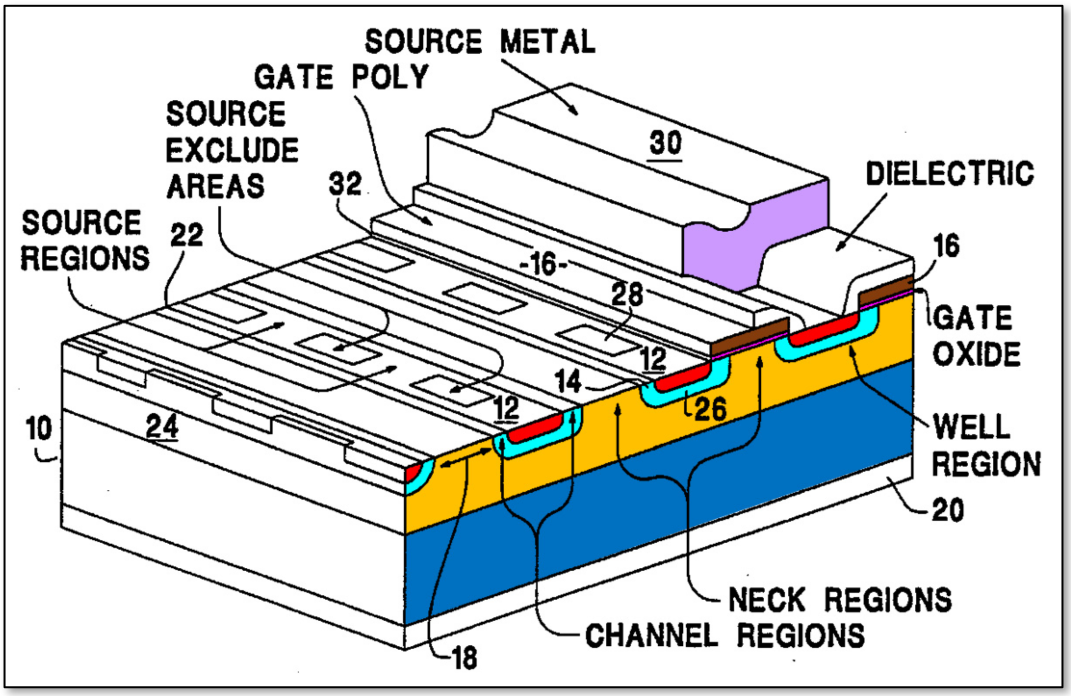
EX1003, FIG. 2A.

MOSFETs may have cross sections that are the same as or similar to the example shown in *Grant*'s Figure 1.11, *Baliga*'s Figure 1, and *Ryu*'s Figure 2A, yet have different—though all well-known—three-dimensional cellular structures. *See* EX1016, 338–339 ("the DMOS structure allows any conceivable cell topology as long as it meets all technological constraints such as alignment tolerances"); *id.*, Figures 6.55 and 6.56; EX1019, 15–17, 70–73, 455–457. Such cellular structures may include shapes that are hexagonal, square, circular, linear, or triangular. For example, *Grant*'s Figure 1.13 (reproduced below) illustrates two cellular structures—hexagonal and square—that have similar cross sections. EX1002, ¶43.



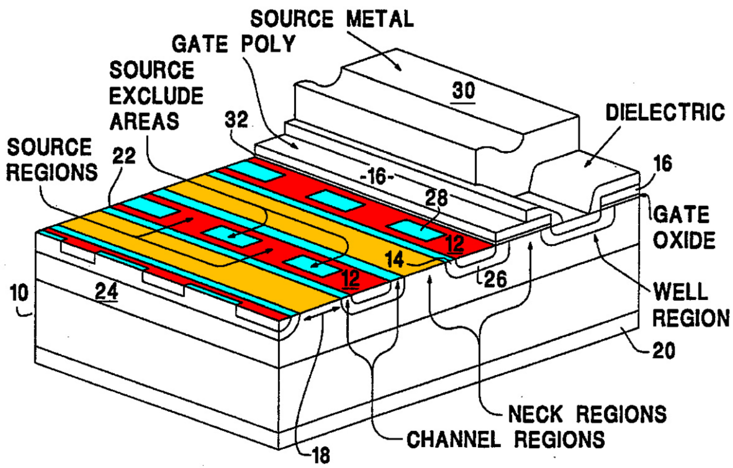
EX1019, Figure 1.13 (annotated)

Figure 1 (reproduced below) of U.S. Patent No. 5,317,184 ("*Rexer*") (EX1015) shows a three-dimensional linear cellular design of a MOSFET that also has a similar cross section to those in *Grant*'s Figure 1.13 but a linear shape to its cellular structure. EX1002, ¶44.

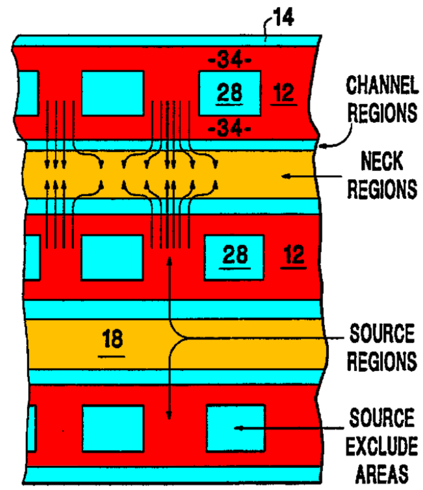


EX1015, FIG. 1 (annotated)

Top or plan views of power MOSFETs may also be shown. For example, *Rexer* illustrates, in Figure 2, a partial plan view of the surface 22 of its MOSFET of Figure 1, "with the gate oxide, gate, and source metal removed." EX1015, 1:43–45, 2:34–36. In *Rexer*'s Figure 2, the linear cellular structure is shown extending left-to-right in the plan view. EX1002, ¶45.



EX1015, FIG. 1 (annotated)



EX1015, FIG. 2 (annotated)

Williams shows top views of other known MOSFET features. For example, *Williams*'s Figure 19E shows a linear cellular structure extending top-to-bottom. EX1002, ¶46.

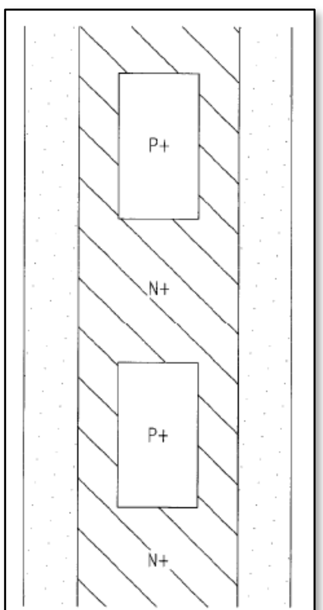


FIG. 19E

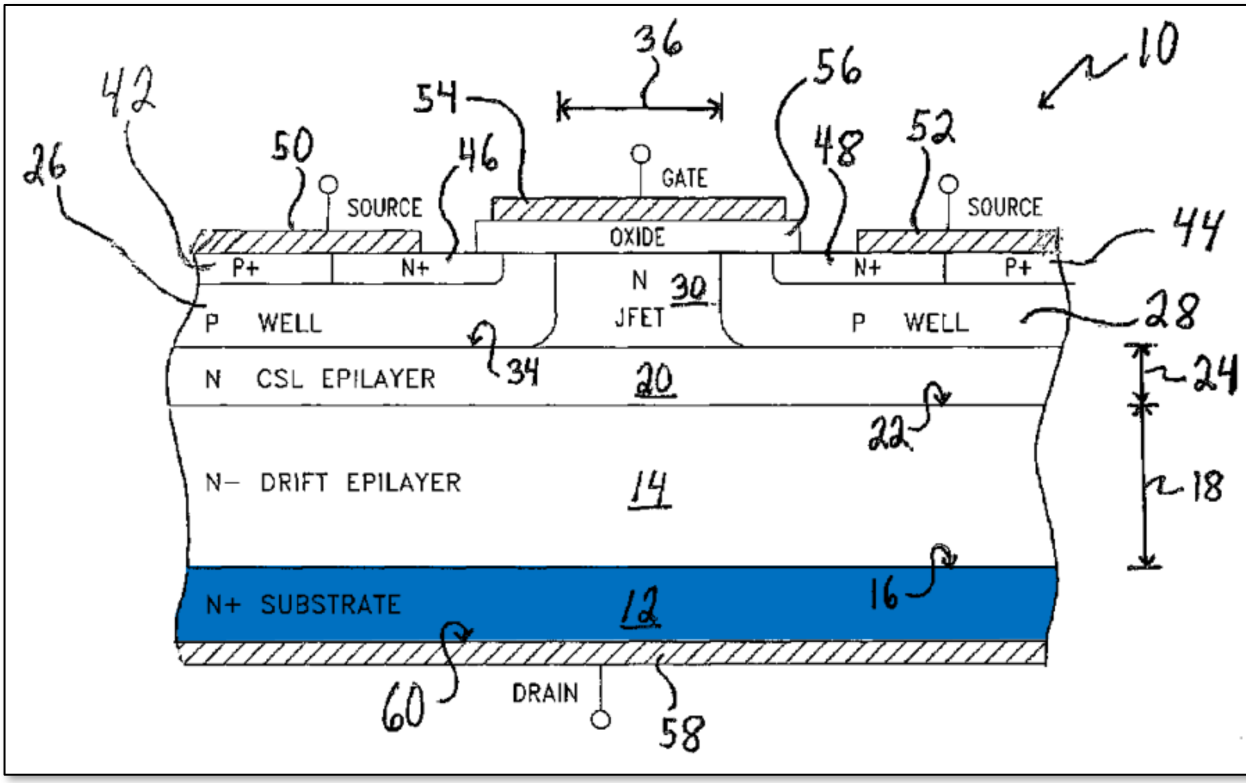
EX1004, FIG. 19E

The relationships between cross-sectional, perspective, and top views of MOSFETs were well known. A POSITA would have understood that, if a cross-sectional view of a unit cell of a MOSFET like shown in *Ryu*'s Figure 2A were of a linear cellular design like in *Rexer*, then *Ryu*'s cellular structure would extend perpendicular to the page just like the structure shown in *Rexer*'s Figure 1. Similarly, a POSITA would have recognized that a top view like shown in *Williams*'s Figure 19E would extend in the same longitudinal direction as the top side of *Rexer's* three-dimensional MOSFET. EX1002, ¶47.

VII. OVERVIEW OF THE '633 PATENT

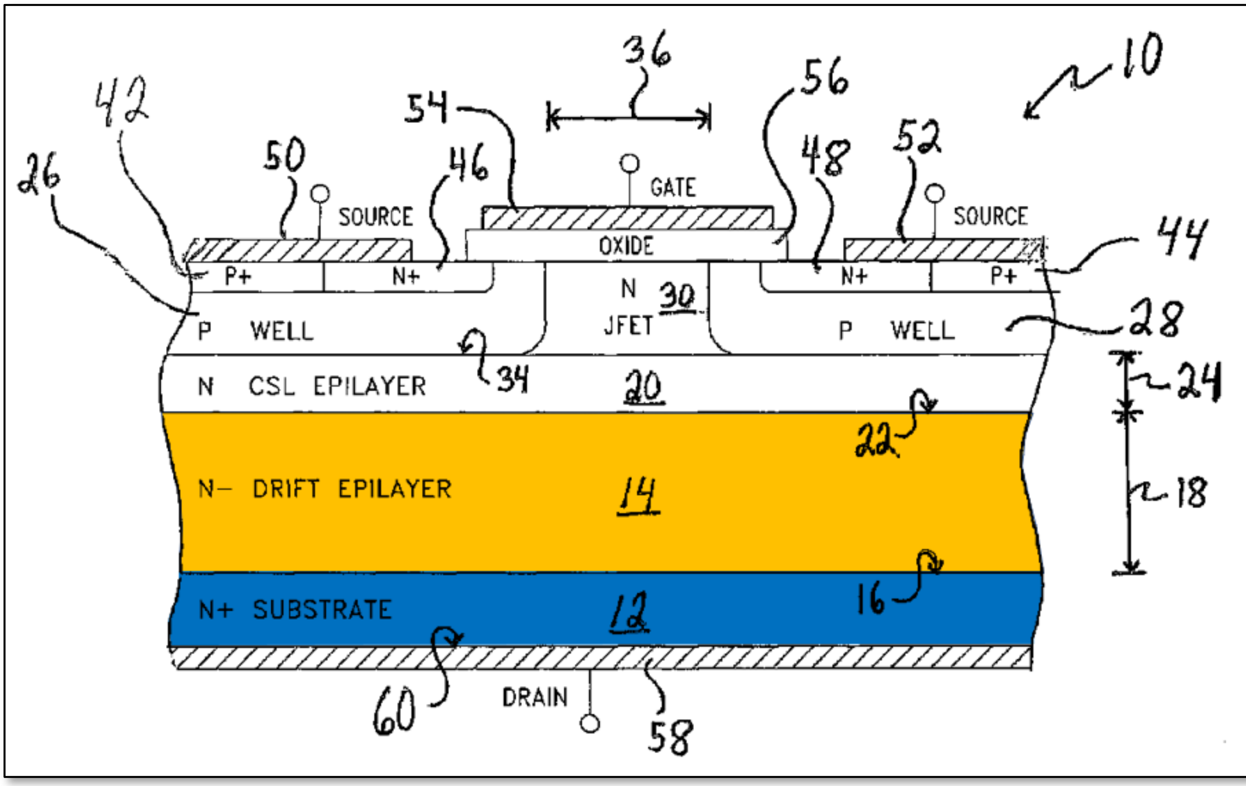
A. Alleged Invention

The '633 patent is directed to semiconductor devices for high-voltage power applications, in particular a "vertical double-implanted metal-oxide semiconductor field-effect transistor." EX1001, 1:12-14, 3:7–8, 4:4-9, Figure 1. As the '633 patent's Figure 1 shows, the semiconductor device 10 includes a **substrate 12** (annotated in blue below) that can be formed from silicon-carbide material and doped with N-type impurity to an "N+" concentration. EX1001, 4:4–13. EX1002, ¶48.



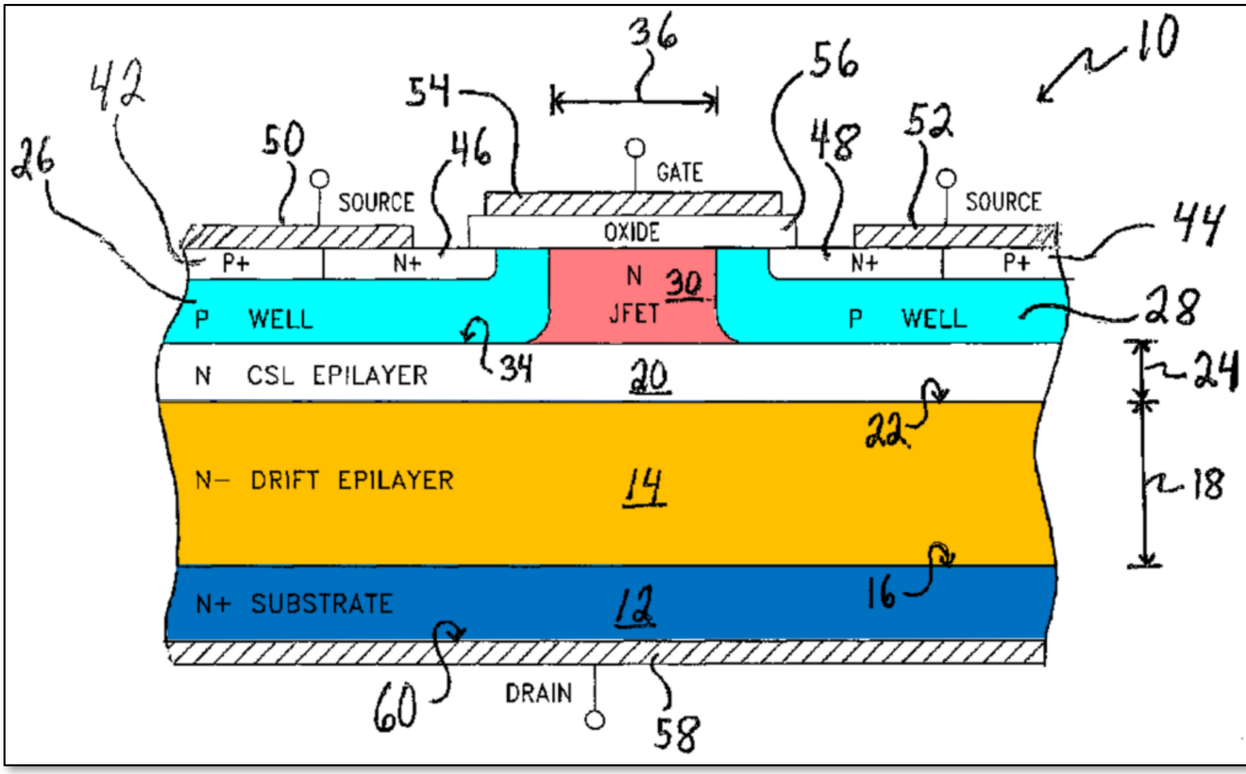
EX1001, FIG. 1 (annotated)

The semiconductor device 10 also includes a **drift layer 14** (annotated in orange below) formed on a front side 16 of the **substrate 12**. *Id.*, 4:20–21, 4:35–41. Not relevant to this petition, the '633 patent's Figure 1 also shows an optional current spreading layer 20 ("CSL"). EX1002, ¶49.



EX1001, FIG. 1 (annotated)

"The semiconductor device 10 also includes two doped semiconductor **wells or base regions 26, 28**" that "are doped with a P-type impurity to a 'P' concentration." *Id.*, 5:23–24, 5:42–43. The region between the **wells 26 and 28** represents the **JFET region 30** (annotated in salmon below). *Id.*, 5:25–26, 6:3–5. The **JFET region 30** and the CSL 20 have similar doping concentrations (*i.e.*, "N" concentration). *Id.*, 5:54–56, Figure 1. EX1002, ¶50.

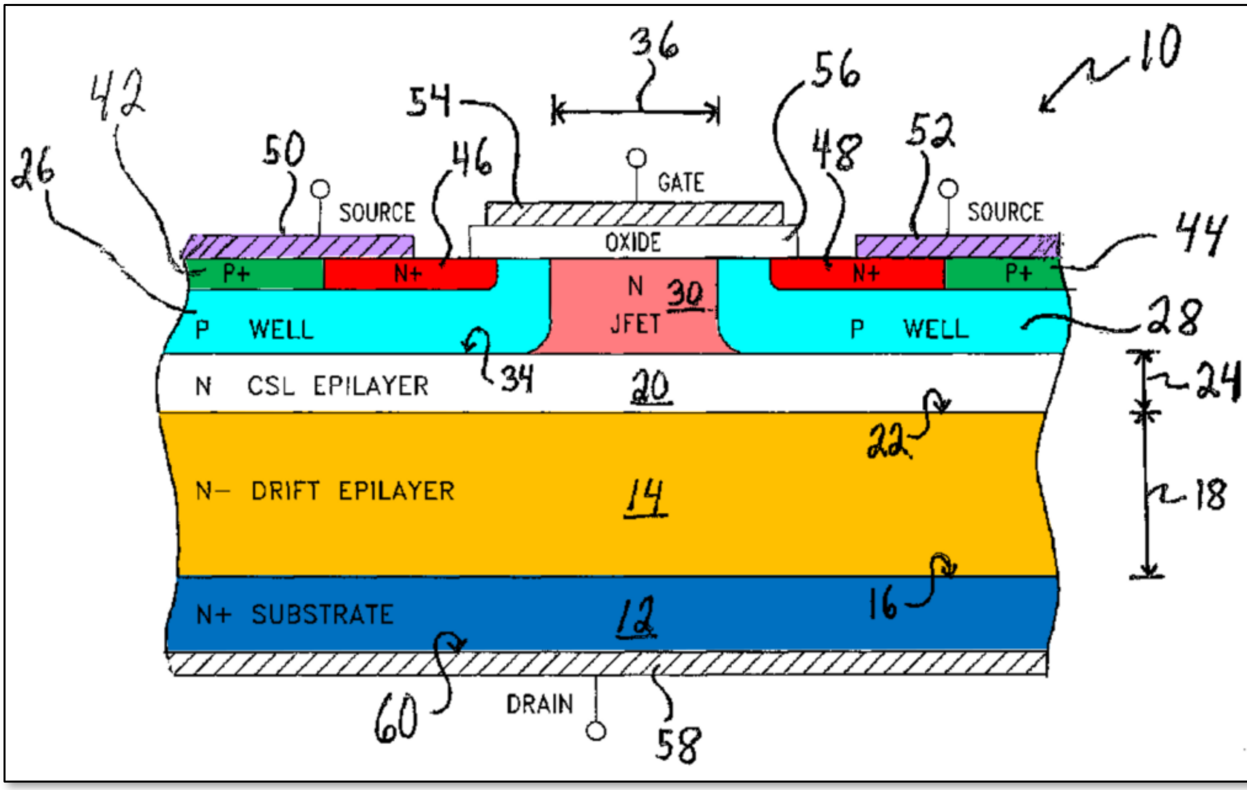


EX1001, FIG. 1 (annotated)

"By forming a JFET region 30 with a doping concentration that is greater than the doping concentration of the drift layer 14, the specific on-resistance of the semiconductor device 10 may be reduced compared to a MOSFET device having JFET regions and drift layers of substantially equal impurity concentrations." *Id.*, 6:16–21; *cf.* EX1019, 83–84 ("Increasing the donor doping concentration in the drain throats . . . has two beneficial effects . . . cell size can be reduced and . . . ***lower*** ***$R_{DS(on)}$ can be realized***."). The '633 patent also explains that fabricating the JFET region 30 to have a width 36 of "three micrometers or less . . . may reduce the specific on-resistance of the semiconductor device 10." *Id.*, 6:21–26; *cf.* EX1019,

83–84 (“Increasing the donor doping concentration in the drain throats . . . has two beneficial effects . . . ***cell size can be reduced*** and . . . lower $R_{DS(on)}$ can be realized.”). EX1002, ¶51.

The device also includes N-type **source regions 46, 48** (annotated in red below) “defined in the P **wells 26 and 28**, respectively.” EX1001, 6:63–66. P-type **base electrode regions 42, 44** (annotated in green below and alternately referred to as “base contact regions” in the ’633 patent specification) are located beside **source regions 46, 48**, respectively. *Id.*, 6:66–7:2; 7:30. As Figure 1 illustrates, metallic **source electrodes 50, 52** (annotated in lavender below) are formed over the **source regions 46, 48**, respectively, and also extend over the **base electrode regions 42, 44**. *Id.*, 7:4-6. EX1002, ¶52.



EX1001, FIG. 1 (annotated)

The ’633 patent describes a “topological configuration” that, “can result in an undesirable source resistance if the **source regions 46, 48** are misaligned with respect to the **base contact regions 42, 44** and/or the **source regions 46, 48** are misaligned with respect to the **source electrodes 50, [52]**.” *Id.*, 7:39–44, Figure 2. To reduce such misalignment the ’633 patent describes other embodiments having source regions that each include “a plurality of base contact regions” arranged to increase “the tolerance to manufacturing variability.” *Id.*, 7:52–8:6. EX1002, ¶53.

Figure 3 shows that “the **base contact regions 158, 160** are embodied as small ‘islands’ or regions within the larger **source regions 154, 156**.” EX1001, 7:57–59.

In this arrangement, the "**base contact regions 158, 160** are formed to be located in a central location under the **source metallic electrodes 50, 52** with areas of **source regions 154, 156** spaced between each **base contact regions 158, 160**." *Id.*, 7:59–63. For the sake of illustration, the annotated Figure 3 below shows the "islands" of **base contact regions 158, 160** as if they are visible in the plan (or top) view; however, it is understood that **source electrodes 50, 52** would cover **base contact regions 158, 160** in the physical device such that the "islands" would not be visible in the plan view (as denoted by dashed lines in the original Figure 3). EX1002, ¶54.

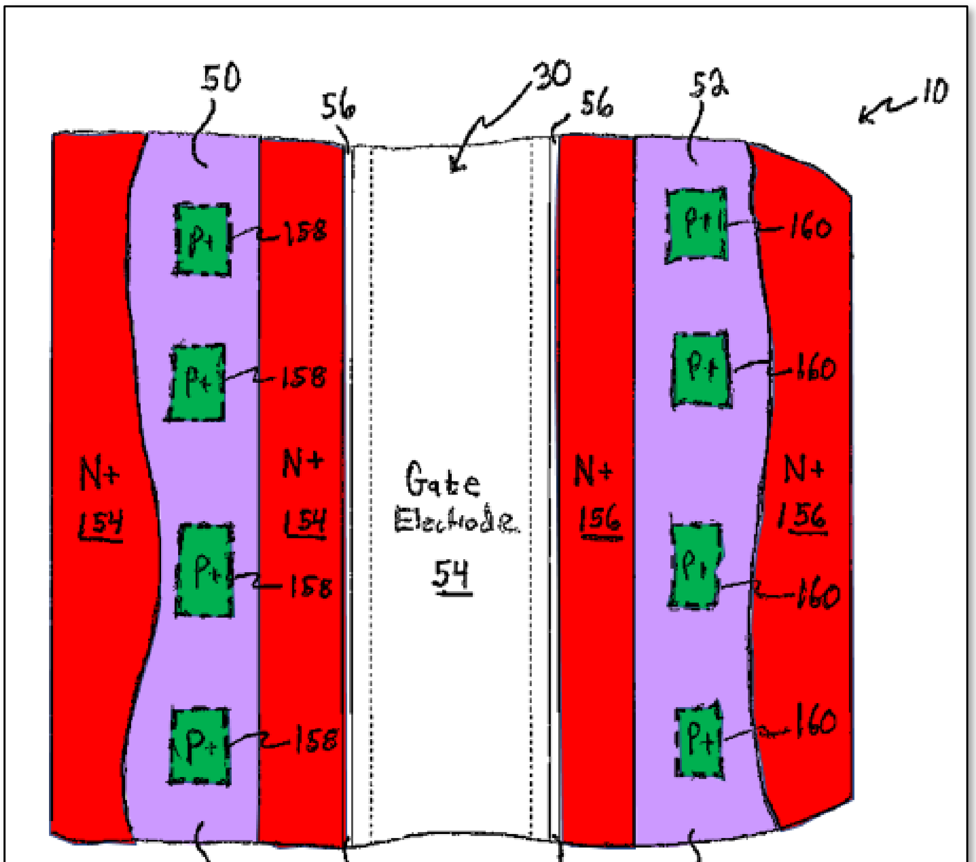


Fig. 3

EX1001, FIG. 3 (annotated)

As demonstrated below, the challenged claims were well-known in the art before the '633 patent's priority date. EX1002, ¶55.

B. Prosecution History

The Examiner issued a non-final Office Action on April 4, 2007, rejecting all originally-filed claims 1–23[3] as being either anticipated by or obvious over several prior art references. EX1008, 2–15. In response, Applicant amended independent claims 1 and 12 to require a silicon-carbide substrate, and claims 12 and 17 to be respectively directed to specific topological configurations of the '633 patent's Figures 3 and 4. EX1009, 2–6. Applicant argued in relevant part that, because "Ono and Zeng are directed toward MOSFET device having silicon substrates, while Kumar is directed toward silicon-carbide MOSFET devices, . . . it is clear that no one of ordinary skill in the art would combine Ono or Zeng with Kumar." *Id.*, 9–10. As explained further below, Petitioner disagrees with the argument Applicant advanced. A POSITA would have been motivated to modify prior art SiC references based on teachings regarding silicon structures. *See* EX1005, 4:22–38 ("Almost all power MOSFETs being marketed today are fabricated in monocrystalline silicon. . .

[3] Pending independent claims 1, 12, and 17 correspond to issued claims 1, 9, and 12, respectively.

. A power MOSFET . . . can be readily translated into silicon carbide using known manufacturing techniques.”).

Correctly unpersuaded by Applicant’s argument, the Examiner issued a final Office Action, rejecting all pending claims and noting that, because “Ono and Zeng disclose ***the structure of the DMOS device*** and Kumar teaches the alternative of silicon-carbide with its known advantages[,] one of ordinary skill would indeed consider whether their particular problem would call for silicon-carbide.” EX1010, 12. Applicant responded with similar arguments, but also further amended claims 12 and 17. *See* EX1011, 2–9.

The Examiner rejected claim 1, maintaining that a POSITA would combine silicon and SiC references, and allowed claims 12 and 17. EX1012, 2, 9–10. The Examiner also indicated the allowability of claim 1’s dependent claim 11, which was directed to the same topological configuration as claim 17. EX1012, 9. Thereafter, Applicant amended claim 1 to include the subject matter of claim 11. EX1013, 2, 8. The Examiner subsequently issued a Notice of Allowance. EX1014, 2.

The Examiner did not have the benefit of *Ryu* and *Williams*, which are not of record. As this Petition demonstrates, *Ryu* and *Williams* render obvious the allegedly inventive features of the ’633 patent, including the configuration recited by issued claim 9 and its dependents. EX1002, ¶60.

VIII. PRIOR ART PATENTS AND PUBLICATIONS

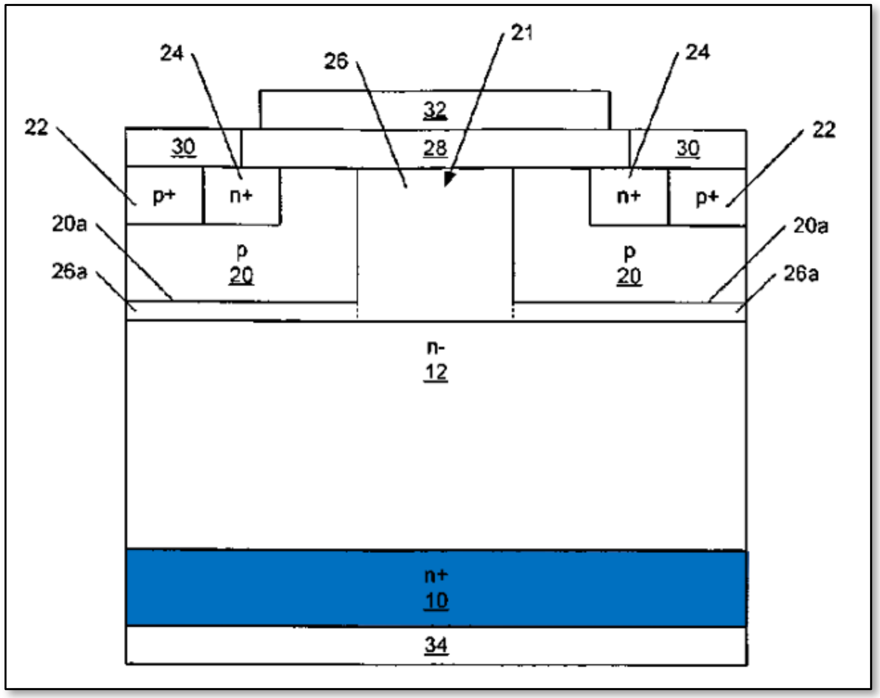
The following references are pertinent to the ground of unpatentability:

A. *Ryu*

U.S. Patent Application Publication No. 2004/0119076 to Ryu ("*Ryu*") (EX1003) was filed on October 30, 2003 and published on June 24, 2004. *Ryu* is prior art at least under 35 U.S.C. §§ 102(a) and 102(e). *Ryu* was not of record in the '633 patent's prosecution history.

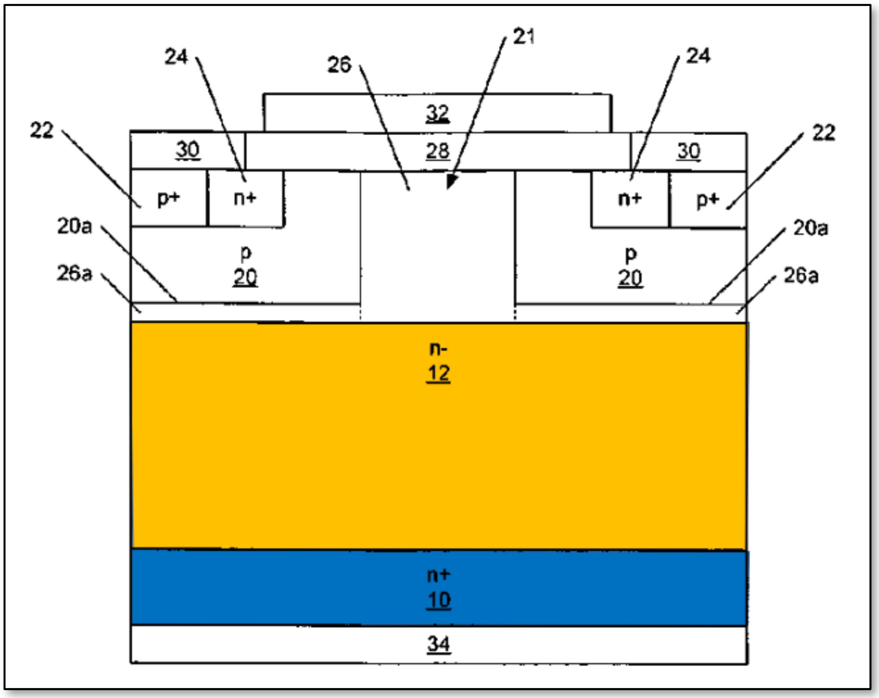
Like the '633 patent, *Ryu* relates to "semiconductor devices . . . and, more particularly, to silicon carbide (SiC) metal-oxide semiconductor field effect transistors (MOSFETs)." EX1003, ¶3. Also like the '633 patent, *Ryu*'s embodiments of SiC MOSFETs "may reduce on-state resistance." *Id.*, ¶¶39, 64, 65. EX1002, ¶62.

Ryu's Figure 2A (reproduced below) shows a cross-sectional view of an embodiment of *Ryu*'s vertical MOSFET, which, as explained below, is strikingly similar to the cross-sectional view of the '633 patent's MOSFET. EX1003, ¶¶28, 40. In *Ryu*'s Figure 2A, **layer 10** (annotated in blue below) may be a substrate made of SiC and doped to an "n+" concentration. *See id.*, ¶40. EX1002, ¶63.



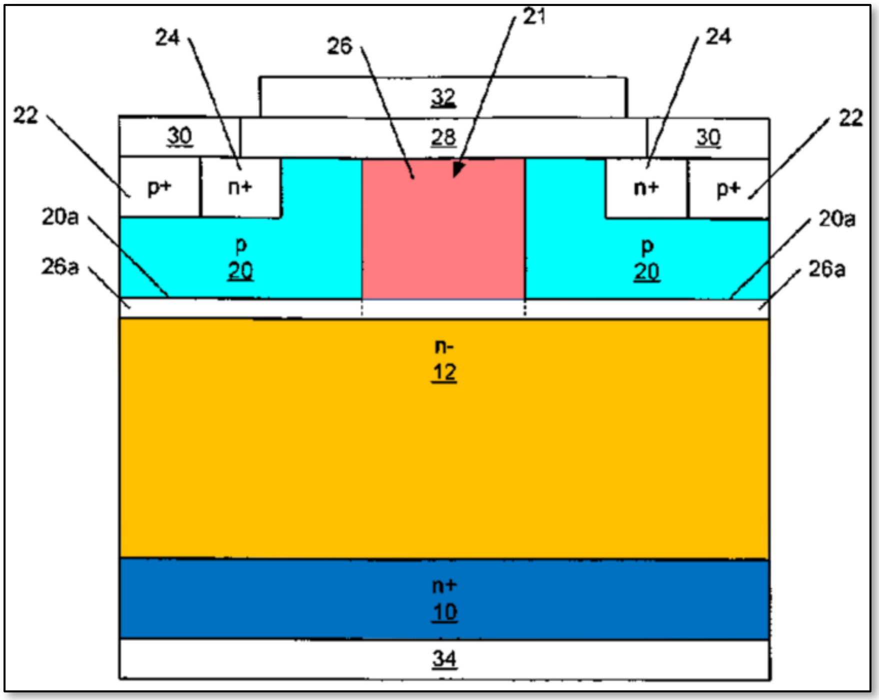
EX1003, FIG. 2A (annotated)

Ryu's MOSFET further includes a **drift layer 12** (annotated in orange below) on the substrate **layer 10**. EX1003, ¶40. Like in the '633 patent, the **drift layer 12** may be an epitaxial layer of SiC and doped to an "n–" concentration. *Id.* EX1002, ¶64.



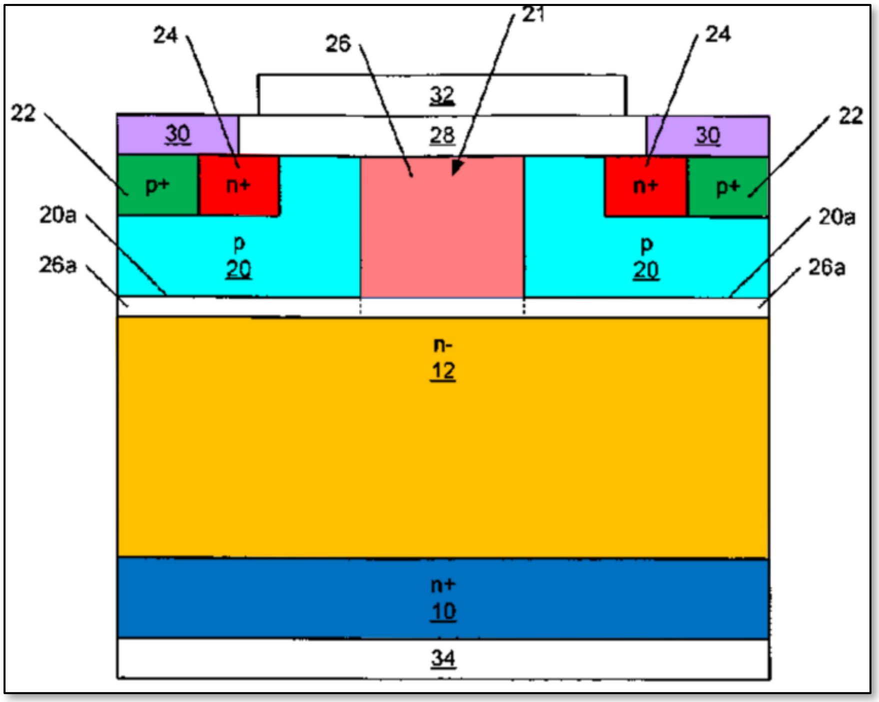
EX1003, FIG. 2A (annotated)

The gap between the **p-wells 20** "may be referred to as the **JFET region 21**" (annotated in salmon below). EX1003, ¶44. *Ryu* points out that "the gap 21 [(*i.e.*, the **JFET region 21**)] between the **p-wells 20** has a higher carrier concentration than the **drift layer 12**." *Id.*, ¶42. According to *Ryu*, "if the gap is too narrow, the resistance of the **JFET region 21** may become very high." EX1003, ¶44. For this reason, *Ryu* discloses that "gaps of from about 1 μm to about 10 μm are preferred." *Id.* EX1002, ¶65.



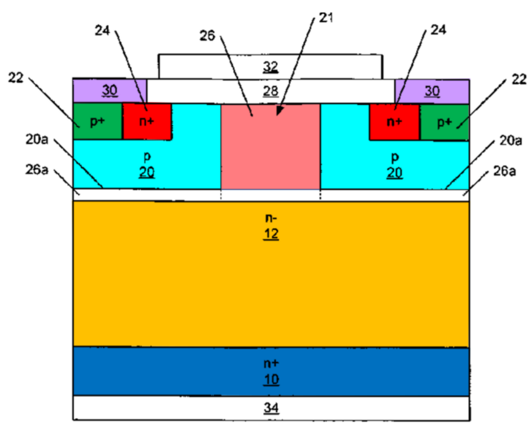
EX1003, FIG. 2A (annotated)

Ryu's MOSFET also includes **n+ regions 24** (annotated in red below) and **p+ regions 22** (annotated in green) disposed within the **p-wells 20**. EX1003, ¶45. The **n+ regions 24** are doped with n-type dopants to a "n+" concentration. *Id.*, ¶¶6, 45, and Figure 1. The **p+ regions 22** are adjacent to the **n+ regions 24** and formed by implanting p-type impurities to a "p+" concentration. *Id.*, ¶55. *Ryu* further discloses **source contacts 30** (annotated in lavender) "to provide an ohmic contact to both the **p+ regions 22** and the **n+ regions 24**." EX1003, ¶47. EX1002, ¶66.

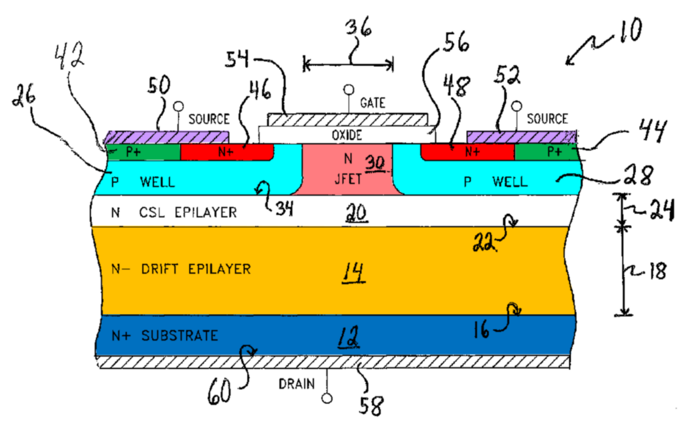


EX1003, FIG. 2A (annotated)

Comparing *Ryu*'s Figure 2A with the '633 patent's Figure 1 reveals that that *Ryu* discloses the same relevant semiconductor structure as the '633 patent. EX1002, ¶67.



EX1003, FIG. 2A (annotated)



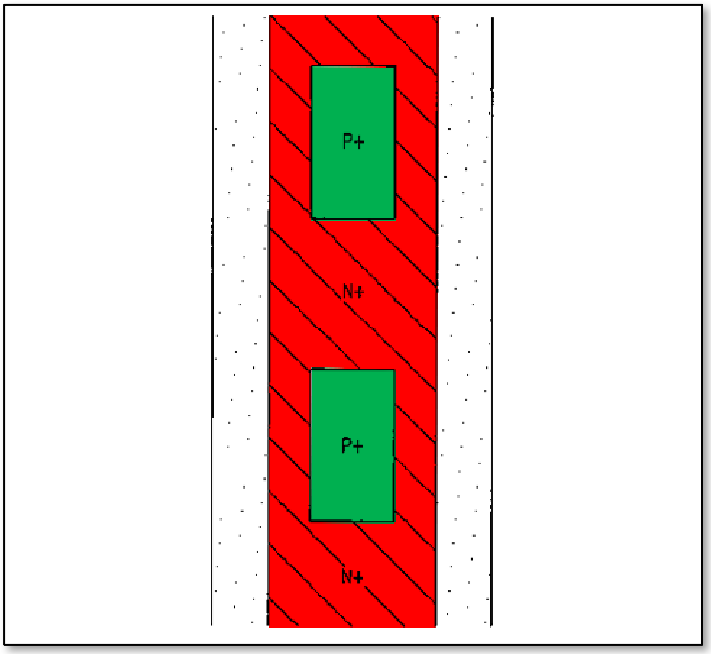
EX1001, FIG. 1 (annotated)

B. *Williams*

U.S. Patent No. 6,413,822 ("*Williams*") (EX1004) issued on July 2, 2002, and is prior art under at least 35 U.S.C. § 102(b). *Williams* is not of art-of-record.

Like the '633 patent, *Williams* relates to vertical MOSFETs. *See, e.g.*, EX1004, 1:7–8, Figure 1. *Williams* notes that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." *Id.*, 1:50–52. One of these resistive constituents is the source contact resistance. *See id.*, 1:33–37. *Williams* discloses "plan views of various source-body designs" in Figures 19A–19F—including plan views just like those of the '633 patent—to "achieve the lowest possible resistance" by maximizing the area of the **N+ source regions** and/or to "suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device" (*i.e.*, prevent unwanted activation of the parasitic bipolar transistor) by maximizing the contact of the **P+ body contact regions** to the body region. *Id.*, 10:17–18; 16:28–35. EX1002, ¶68.

Like the '633 patent's source regions 154, 156 with "island" base contact regions 158, 160, *Williams* also discloses a continuous **N+ source region** (annotated in red below) with **P+ body contact windows** (annotated in green) in Figure 19E. EX1004, 10:23–24; EX1001, Figure 3. *Williams* teaches that such a source-body design provides "better **N+** contact resistance and less **P+** contact area (less rugged)." EX1004, 17:18–19. EX1002, ¶69.



EX1004, FIG. 19E (annotated)

IX. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard." *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board need only construe the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, given the close correlation between the asserted prior art and the challenged claims of the '633 patent, the Board need not construe any terms of the challenged claims to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a POSITA

at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.[4]

X. SPECIFIC GROUND FOR UNPATENTABILITY

Under 37 C.F.R. § 42.104(b)(4)–(5), the following sections (as confirmed in Dr. Subramanian's declaration, EX1002, ¶¶70–143) detail the ground of unpatentability, the limitations of challenged claims 9–11 of the '633 patent, and how these claims are therefore obvious in view of the prior art. EX1002, ¶¶70–143.

A. Ground I: Claims 9–11 are Obvious Over *Ryu* in View of *Williams*

1. Independent Claim 9

a) 9[preamble]: "A double-implanted metal-oxide semiconductor field-effect transistor comprising:"

Regardless of whether the preamble is limiting, *Ryu* discloses it. *Ryu* discloses a metal-oxide semiconductor field-effect transistor (MOSFET). EX1003, ¶¶3, 28, 40. *Ryu* explicitly states that Figure 2A is a MOSFET. *Id.*, ¶40 ("MOSFETs according to embodiments of the present invention are illustrated in FIG. 2A."). *Ryu*'s Figure 2A is reproduced below, alongside the '633 patent's Figure 1 for comparison. EX1002, ¶72.

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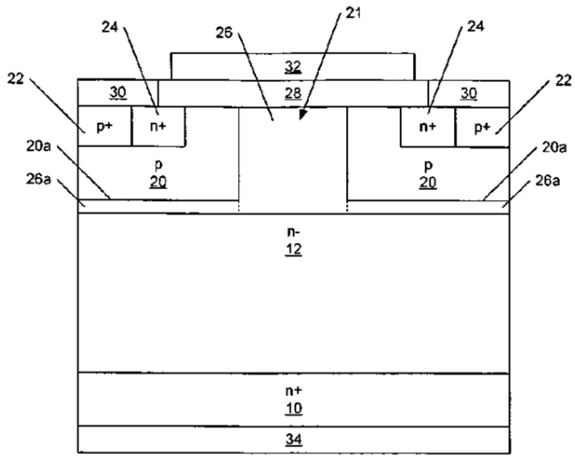
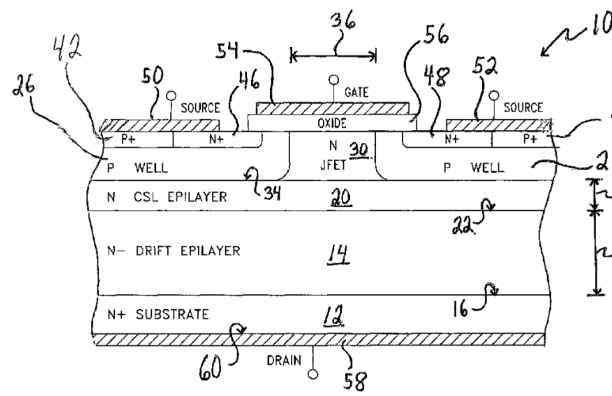
[4] Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as relevant and appropriate.



EX1003, FIG. 2A



EX1001, FIG. 1

Ryu's MOSFET includes a gate contact 32 ("the gate contact is ***metal***"; EX1003, ¶13; *see also id.*, claims 10 and 41), over a gate oxide 28 ("The gate oxide may be thermally grown and may be a nitrided ***oxide*** and/or may be other oxides."; *id.*, ¶46), over a combination of silicon carbide (*i.e.*, a ***semiconductor***) layers 26, 12, and 10 (*id.*, ¶¶40–41), thereby creating a metal-oxide semiconductor device. *Cf.* EX1005, 1:45–50 (describing a MOSFET as including "a conducting gate electrode, typically metal, that is separated from a semiconductor surface by an intervening insulator, typically silicon dioxide."). EX1002, ¶73.

Ryu's MOSFET is doubly implanted. *Ryu* explains that, during the fabrication process of its MOSFET, using a mask 100, "impurities are implanted into the n-type epitaxial layer 26 to provide the p-wells 20," and in the next step of the process, "n-type impurities are implanted utilizing the mask 104 to provide the n+ regions 24." EX1003, ¶¶ 53–54, Figures 4B and 4C; *cf.* EX1021, 1:56–63 ("***double ion implantation sequence*** . . . by successive ion implantation of an acceptor atom (such

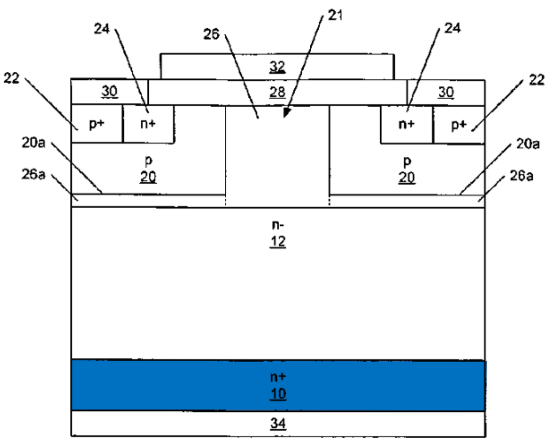
as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) ***to form the base and source regions***, respectively."); EX1020, 960 ("DMOS structure is formed in SiC using a ***double ion implantation with two separate implantation masks***."); EX1022, 659. *Ryu*'s doubly implanted p-wells 20 and n+ regions 24 configuration is also the same as in the "Vertical ***Doubly Implanted MOSFET*** (DIMOSFET)" that *Ryu* illustrates in Figure 1. EX1003, ¶¶6, 27, Figure 1. EX1002, ¶74.

Therefore, *Ryu*'s MOSFET corresponds to the '633 patent's "*double-implanted metal-oxide semiconductor field-effect transistor*." EX1002, ¶75.

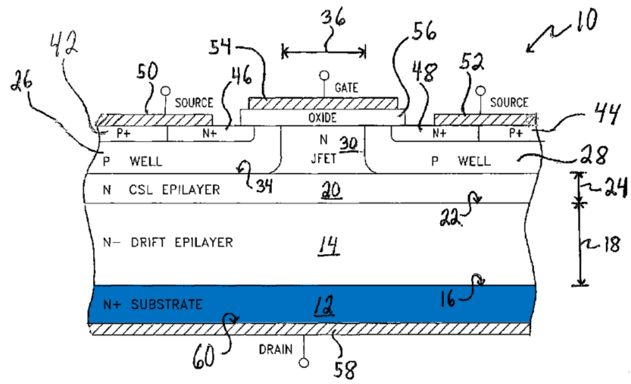
b) 9[a]: "a silicon-carbide substrate;"

Ryu discloses element 9[a]. *Ryu* explains that its **layer 10**, which is shown in various figures such as Figures 2A, 2B, 3, and 4E, is made of silicon carbide. For example, *Ryu* states that "…layer 12 of silicon carbide is on an optional n+ ***layer 10 of silicon carbide***." EX1003, ¶40. *Ryu* also explains that **layer 10** can be the substrate. *Id*., ¶56 ("…***layer 10***, which may be formed by a backside implant of n-type impurities in a substrate or ***may be*** an epitaxial layer or ***the substrate itself***"). *Ryu*'s claims 13 and 23, which were published along with the rest of *Ryu* on June 24, 2004, and therefore qualify as prior art, also clearly disclose a silicon carbide substrate. *Id*., claims 13 ("… comprising an n-type ***silicon carbide substrate***"), 23 ("… wherein the n-type silicon carbide layer comprises an n-type ***silicon carbide***

substrate."). As shown by *Ryu*'s Figure 2A and the '633 patent's Figure 1, both of which are reproduced below, *Ryu*'s silicon carbide substrate 10 corresponds to the '633 patent's silicon carbide substrate 12. EX1002, ¶76.



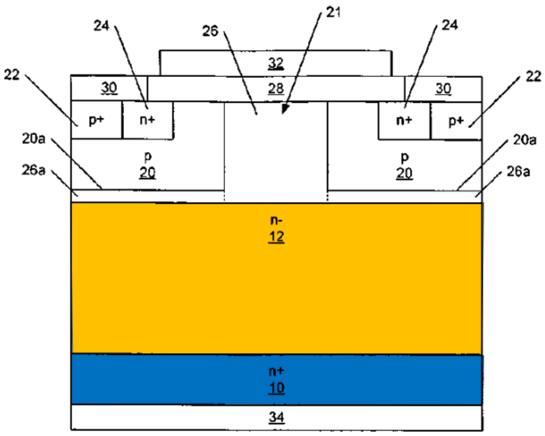
EX1003, FIG. 2A (annotated)



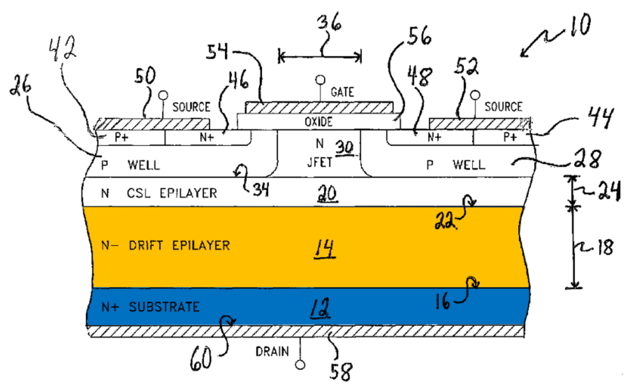
EX1001, FIG. 1 (annotated)

c) 9[b]: "a drift semiconductor layer formed on a front side of the semiconductor substrate;"

Ryu discloses element 9[b]. *Ryu*'s Figure 2A (reproduced below, alongside the '633 patent's Figure 1), shows that "a lightly doped n− **drift layer 12** of silicon carbide" (*i.e.*, *"a drift semiconductor layer"*) is on the n+ **layer 10**. EX1003, ¶40. *Ryu* further explains that its **drift layer 12** is "*formed on a front side of the semiconductor substrate*." *Ryu*'s Figure 2A shows that **drift layer 12** is on the front side of substrate 10, just as the drift layer 14 of the '633 patent is on its substrate 12. *Ryu* also makes clear that its **drift layer 12** is formed on substrate 10. *Id.*, ¶53 ("Alternatively, the drift layer 12 may be ***provided on an n+ silicon carbide substrate***."). EX1002, ¶77-78.



EX1003, FIG. 2A (annotated)



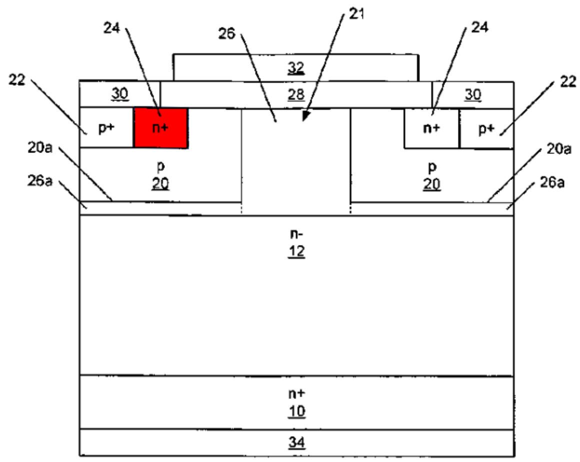
EX1001, FIG. 1 (annotated)

d) 9[c]: "a first source region;"

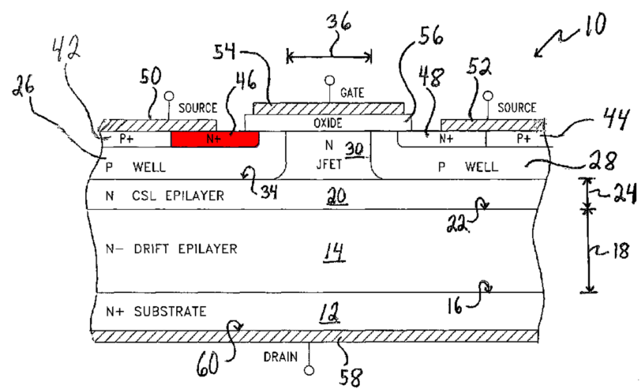
Ryu discloses element 9[c]. *Ryu* discloses that "**regions of n+ silicon carbide 24** . . . are disposed within p-wells 20." EX1003, ¶45. A POSITA would have understood *Ryu*'s **n+ regions 24** to be source regions because *Ryu*'s **n+ regions 24**: (1) are contacted by source contacts 30; and (2) correspond to the same "source regions" both in *Ryu* and *Ryu*'s other articles describing the same structure. EX1002, ¶79.

First, *Ryu* explains that ***source*** contacts 30 provide ohmic contact to the **n+ regions 24**. EX1003, ¶47 ("Source contacts 30 … provide an ohmic contact to … the n+ regions 24."); *see also id.*, claims 6 and 36 ("a source contact on the first n-type silicon carbide region"). A POSITA would have understood that the **n+ regions 24** are ***source*** regions because they are contacted by the ***source*** contacts 30. In the same way, the '633 patent forms "source metallic electrode 50, 52 … over the source regions 46, 48, respectively" to achieve the same function. EX1001, 7:4-6. A

comparison below of *Ryu*'s Figure 2A and the '633 patent's Figure 1 also shows that *Ryu*'s **n+ regions 24** correspond to the '633 patent's **source regions 46 and 48** and are similarly of n-type doping at an "n+" concentration. EX1002, ¶80.

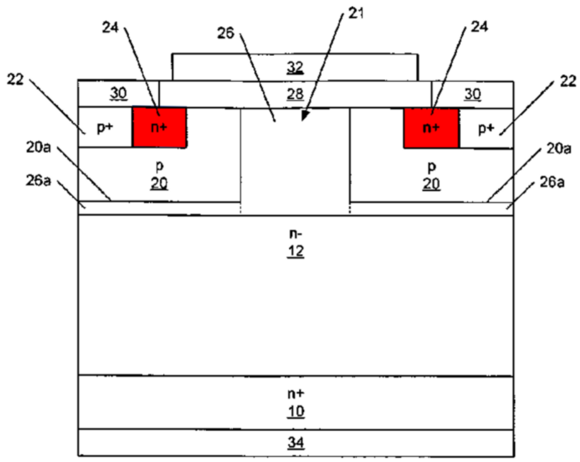


EX1003, FIG. 2A (annotated)

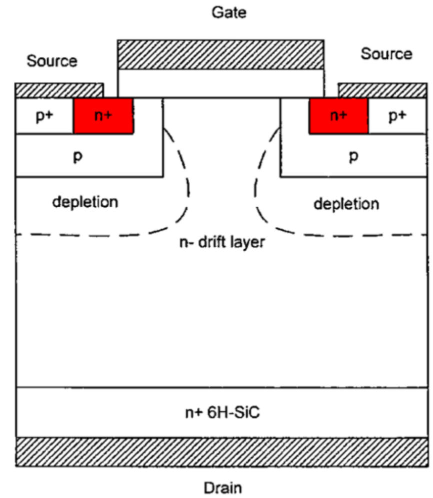


EX1001, FIG. 1 (annotated)

Second, the **n+ regions 24** in *Ryu*'s Figure 2A correspond, in location and in relative position to other structures, to the n+ regions in *Ryu*'s double-implanted MOSFET of Figure 1. EX1003, ¶27 ("FIG. 1 is a cross-sectional view of a conventional ***DIMOSFET***"). *Ryu*'s Figures 1 and 2A are reproduced below with the n+ regions highlighted in red. *Ryu* explicitly discloses that the n+ regions in Figure 1 are "source regions." *Id.*, ¶6 ("***source regions (n+)***"). A POSITA would have understood that the **n+ regions 24** in Figure 2A correspond to the **n+ regions** in *Ryu*'s Figure 1 and that they were all source regions. EX1002, ¶81.

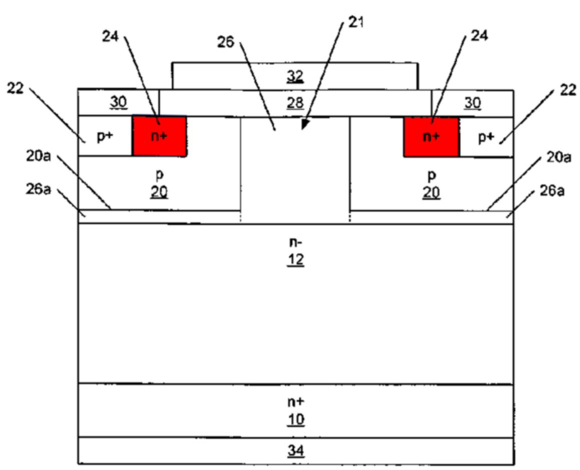


EX1003, FIG. 2A (annotated)

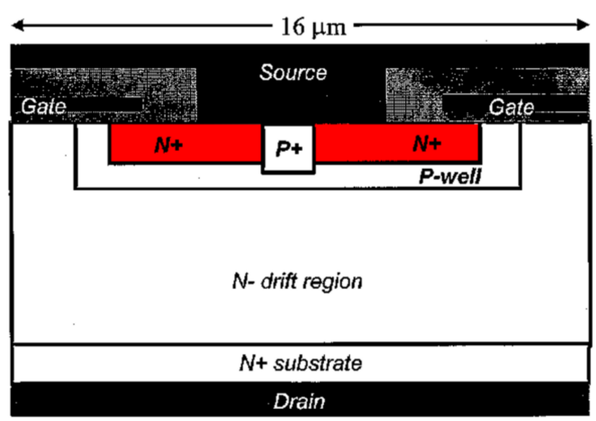


EX1003, FIG. 1 (annotated)

Similarly, the **n+ regions 24** in *Ryu*'s Figure 2A correspond to the N+ regions in the "DiMOSFET" that the inventor of *Ryu* presents in Figure 1 (reproduced below side-by-side with *Ryu*'s Figure 2A, with the N+ regions annotated in red) of a 2002 article titled "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC." EX1023, Figure 1; *see also* EX1024, Figure 2. EX1002, ¶82.



EX1003, FIG. 2A (annotated)



EX1023, FIG. 1 (annotated)

Ryu's articles explicitly disclose that the N+ regions are "source regions." EX1024, 881 (describing "n+ source regions were formed by nitrogen

implantation"); *see also* EX1023, 321 (also describing "***N+ source regions***"). Accordingly, a POSITA would have understood *Ryu*'s **n+ regions 24** in Figure 2A to be ***source*** regions. EX1002, ¶¶83-84.

Thus, for example, *Ryu* discloses at least a first **n+ region 24** (*i.e.*, "*a first source region*") on the left in Figure 2A and a second n+ region 24 on the right. EX1002, ¶85.

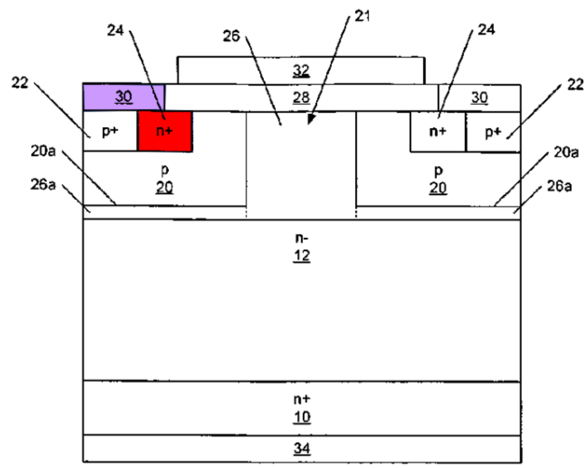
e) 9[d]: "a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;"

The combination of *Ryu* and *Williams* renders element 9[d] obvious. As explained below, *Ryu*'s **source contact 30** is a source electrode that is over **source region 24**. Moreover, it would have been obvious for *Ryu*'s **source contact 30** to define a longitudinal axis. EX1002, ¶86.

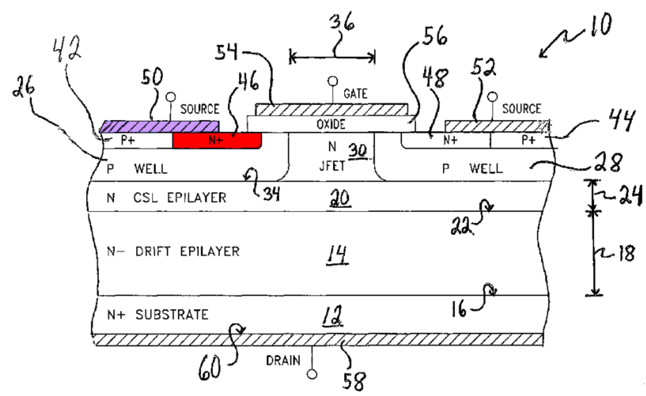
i. "source electrode"

Ryu discloses that "one or more **source contacts 30**, in some embodiments are formed of nickel (Ni), titanium (Ti), platinum (Pt) or aluminum (Al), combinations thereof . . . to provide an ohmic contact to both the p+ regions 22 and the **n+ regions 24**." EX1003, ¶47. Because *Ryu*'s **source contacts 30** are formed from a conductor, and because they physically contact the **n+ regions 24** (*i.e.,* "source regions"), they are "source electrodes." Moreover, *Ryu*'s **source contacts 30** perform the same function as the '633 patent's source electrodes. *Ryu*'s Figure

2A, for example, shows that the **source contacts 30** are over the **n+ regions 24**, just like the '633 patent's **source electrodes 50 and 52** are over the **source regions 46 and 48**. *See also id.*, claims 6 and 36 ("a ***source contact on*** the first ***n-type*** silicon carbide ***region***"). EX1002, ¶87.



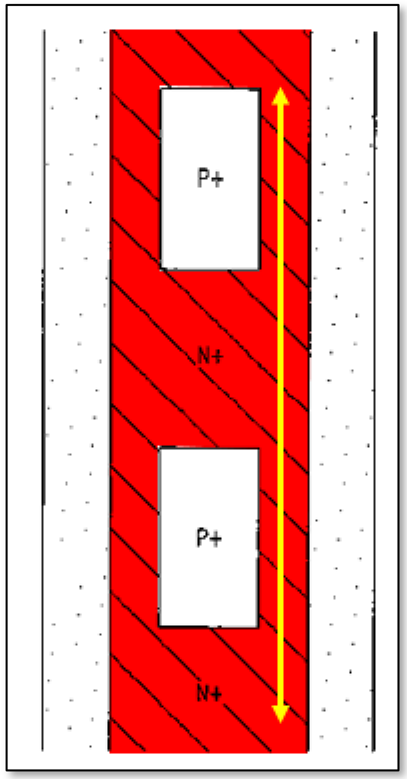
EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

ii. "longitudinal axis"

Ryu in view of *Williams* teaches that the **source contact 30** defines a longitudinal axis. *Williams* discloses vertical MOSFETs having linear cellular configurations. EX1004, Figures 4A, 7A–7B, and 18. Related to these configurations, *Williams* explains that "[t]he source and body contact construction can also be varied geometrically . . . as shown in the plan views of FIGS. 19A–19F." *Id.*, 16:28-30. As shown in *Williams*'s Figure 19E, for example, the **N+ source region** extends along a "*longitudinal axis*" (*i.e.*, up-down with respect to the page), as annotated using a yellow arrow. EX1002, ¶88.



EX1004, FIG. 19E (annotated)

The obviousness of using *Williams*'s linear **N+ source region** configuration, which extends along a longitudinal axis, in *Ryu* is further shown by many other references, as discussed herein, which demonstrate that MOSFETs with linear geometry were notoriously well-known. Moreover, a POSITA would have understood that a source electrode (*e.g.*, a metal or other conductive layer, such as *Ryu*'s **source contacts 30**) would be laid on top of and provide contact to the linear **N+ source region** and that, due to the linear geometry of the **N+ source region**, the source electrode would also extend in the direction of the linear source region and the electrode would thereby define a longitudinal axis. EX1002, ¶89.

As discussed above in Section VI.F, *Ryu*'s Figure 2A is a cross-sectional view of a three-dimensional MOSFET and it was known in the art that such a cross section would correspond to a three-dimensional structure such as any of the well-known hexagonal, square, circular, linear, or triangular cellular structures. *See* EX1016, 338–339 ("the DMOS structure allows any conceivable cell topology as long as it meets all technological constraints such as alignment tolerances"); *id.*, Figures 6.55 and 6.56; EX1019, 15–17, 70–73, 455–457, Figures 1.13 and 3.9. A POSITA would have found it obvious to fabricate *Ryu*'s MOSFET into any one of these known cellular structures and, in particular, the linear cell structure taught by *Williams*. *See, e.g.*, EX1019, 455 ("[O]ne manufacturer advocates the use of a linear metal gate structure … for producing inexpensive high-voltage devices."). EX1002, ¶90.

A POSITA would have understood that, if fabricated as a linear cell, *Ryu*'s cross-sectional view of its MOSFET would extend perpendicularly to the page. The linear cellular arrangement of *Williams* was well-known in the art, as shown by, for example, *Rexer* (at left, below) and Baliga (at right, below), and as explained above, would have been an obvious design choice for *Ryu*'s cellular structure. EX1002, ¶91.

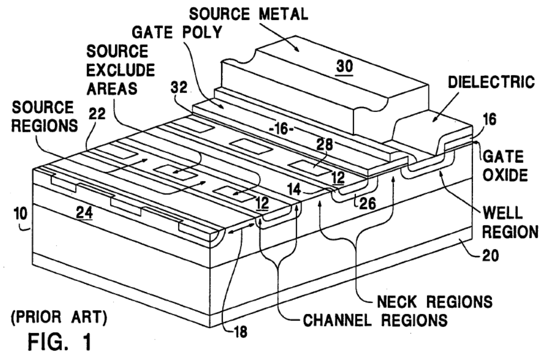


FIG. 1

EX1015, FIG. 1

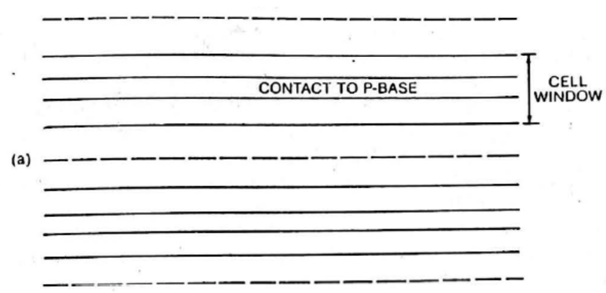


Fig. 6.56. Comparison of linear cell design with (*a*) continuous contact ;

EX1016, FIG. 6.56(a)

Linear cells have been commonly used in semiconductor technology since they have often been the easiest and most reliable structures to pattern lithographically. *See, e.g.*, EX1017, 186 ("One common constraint imposed on VLSI layouts is the "manhattan" property, which requires that every edge of every feature be parallel to either the X or Y axis."); EX1018, 238 ("A typical example of linear placement is the placement of a linear array, such as in gate matrix layout."). Additionally, most layout tools and software for such purposes have made it convenient to draw linear structures. *See, e.g.*, EX1017, 186 ("It can be shown that any complex set of manhattan mask features can be represented exactly in the form of a collection of abutting rectangles. It follows that a layout editor which can manipulate only rectangles can be used to create and edit any manhattan design. Indeed, this approach was taken in early 1980's with the Caesar editor from Berkeley . . ."). As a consequence, linear structures have been overwhelmingly the most common structures used in semiconductor layouts. Additionally, for a device that might be subject to high fields during use, the use of linear cells ensures more

uniform and more predictable fields over the axis of the device. Accordingly, because the linear geometry was well known and because a POSITA would have been motivated to use it, it would have been obvious to construct the MOSFET of *Ryu*'s Figure 2A in view of *Williams*'s teachings of a linear cellular structure such that *Ryu*'s **n+ regions 24** and, consequently, *Ryu*'s **source contacts 30** extended perpendicularly to the page, thereby each **source contact 30** defining a longitudinal axis. EX1002, ¶92.

Thus, *Ryu* in view of *Williams* renders obvious at least a first **source contact 30** (*i.e.*, "*a first source electrode*") on the left, for example, formed over the left **n+ region 24** (*i.e.*, "*the first source region*"), with the first **source contact 30** defining a longitudinal axis. EX1002, ¶93.

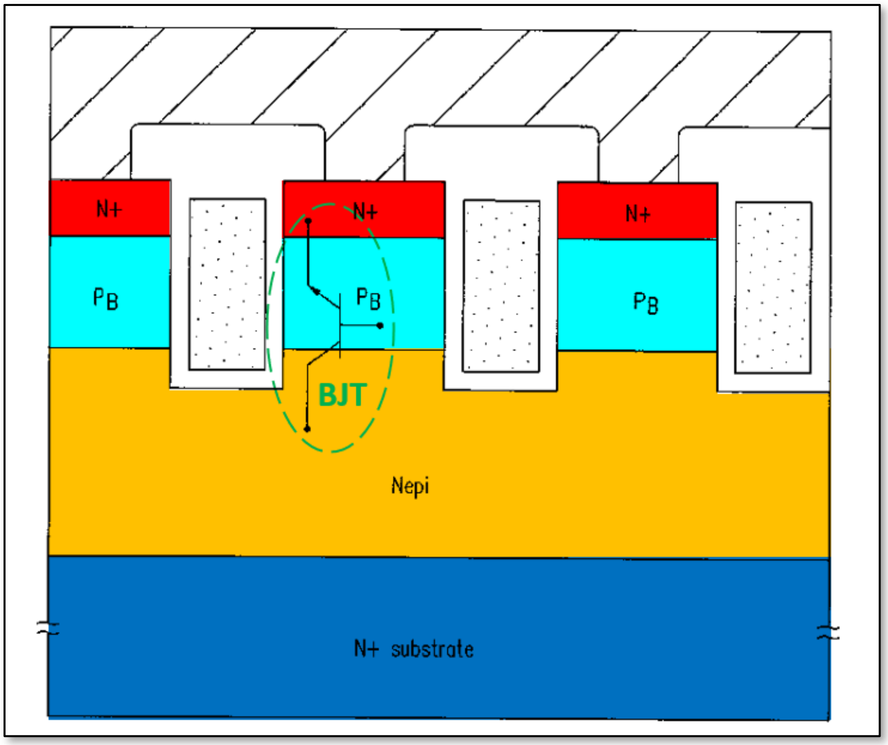
iii. Motivation to Combine Ryu and Williams

A POSITA would have been motivated to implement *Ryu*'s MOSFET according to *Williams*'s teachings such that *Ryu*'s MOSFET was formed using a linear cell structure having the **source contacts 30** define and extend along a longitudinal axis. EX1002, ¶94.

Ryu and *Williams* are from the same field of endeavor. *See, e.g.*, *Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 721 F.2d 1563, 1574–75 (Fed. Cir. 1983); M.P.E.P. § 2141. Both references are directed to vertical MOSFETs. *Ryu* discloses embodiments of vertical MOSFETs that "may reduce on-state resistance" compared

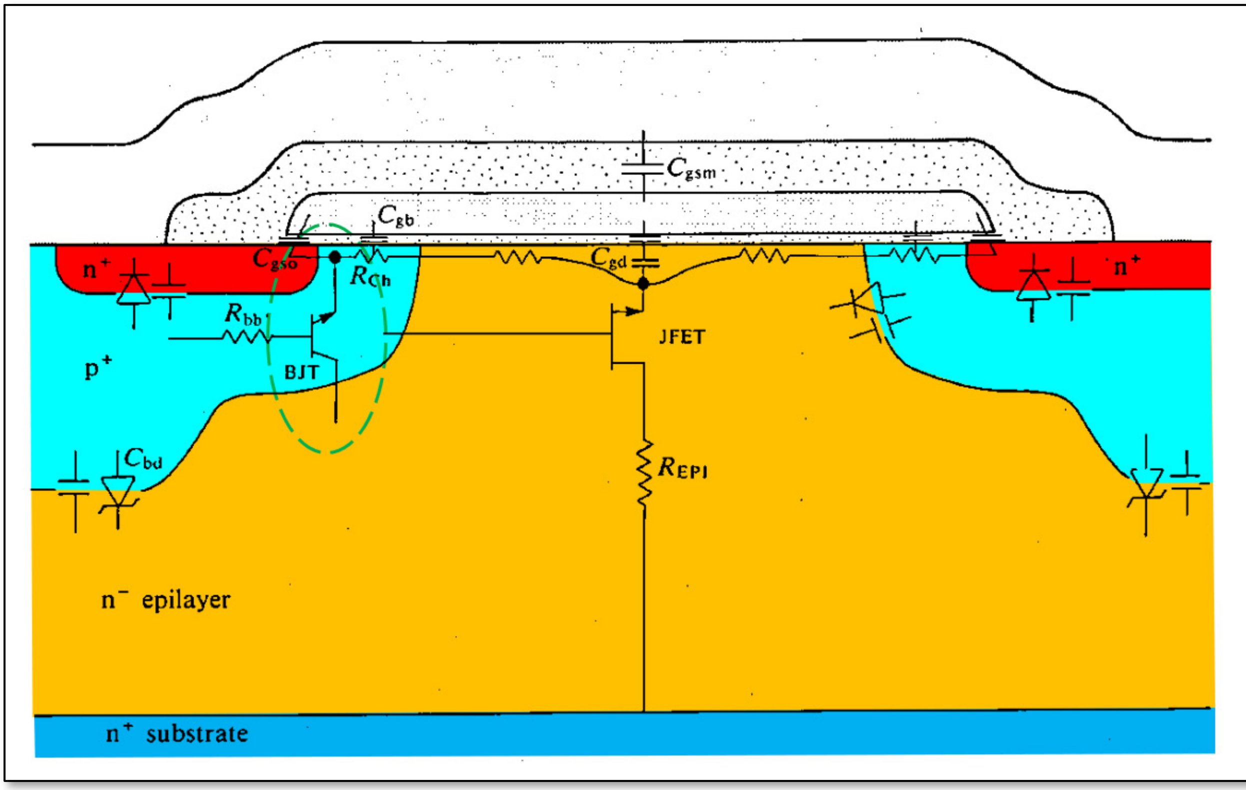
to conventional vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1. *Williams* discloses structures for vertical MOSFETs that are used to reduce on-resistance. *See, e.g.*, EX1004, , Figure 1, 8:15–16 ("reduce the on-resistance of the DMOSFET"), 16:31–32 ("achieve the lowest possible resistance"). Thus, both references are directed to vertical MOSFETs and aim at reducing on-resistance. EX1003, ¶6; EX1004, 1:7–8. EX1002, ¶95.

Although *Williams* discloses MOSFETs with a so-called trench gate and *Ryu* discloses a MOSFET with a so-called planar gate, a POSITA would nonetheless have been motivated to use *Williams*'s teachings in *Ryu*. This is because *Williams*'s and *Ryu*'s MOSFETs share many common features to which the shape of the gate is irrelevant. For example, both *Williams*'s trench-gated vertical MOSFETs and *Ryu*'s non-trench-gated vertical MOSFET include a parasitic BJT within the epilayer that could inadvertently be activated. For both *Williams* and *Ryu*, the solution to the potential problem caused by this parasitic transistor is the same. For example, *Williams* describes such a "parasitic NPN bipolar transistor," which it illustrates in Figure 7A (reproduced below). EX1004, 6:9. EX1002, ¶96.



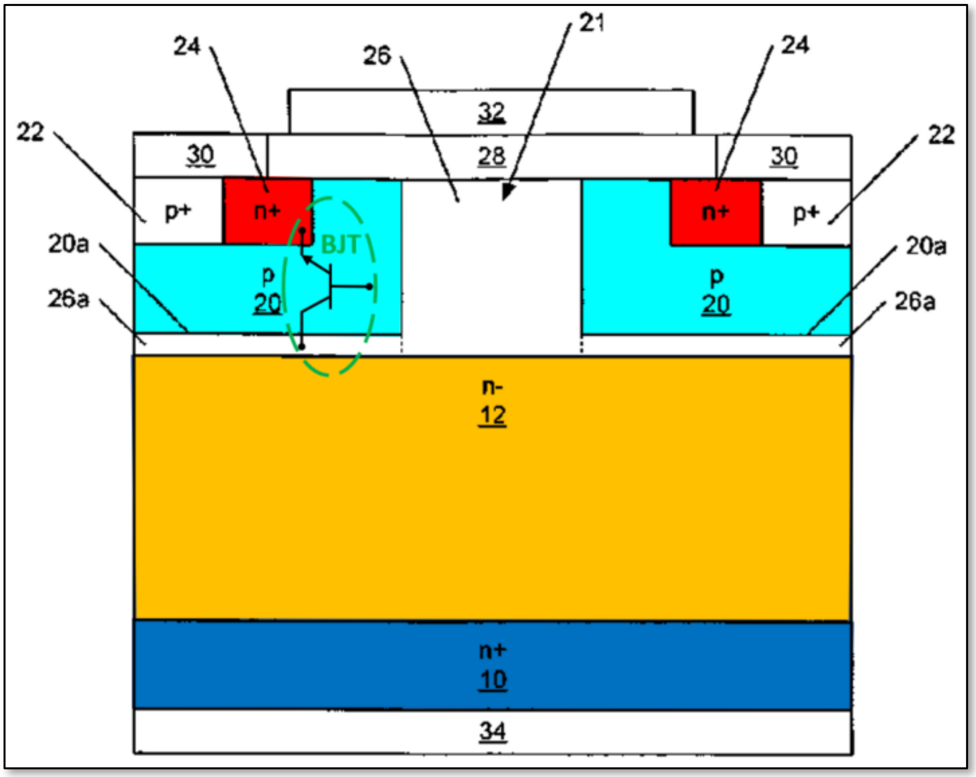
EX1004, FIG. 7A (annotated)

Williams's parasitic BJT is formed between the source, the body, and the drain in the same way *Grant* illustrates a parasitic "npn bipolar junction transistor (BJT) formed between the source, the body, and the drain" of a non-trench-gated vertical MOSFET in Figure 3.15, reproduced below. EX1019, 81. EX1002, ¶97.



EX1019, Figure 3.15 (annotated)

Based on at least *Grant*'s teachings, a POSITA would have understood that a parasitic npn BJT would also be formed in *Ryu*'s MOSFET between the n+ region 24 (*i.e.*, source region), p-well 20 (*i.e.*, body), and the n-type epitaxial layer 26 (*i.e.*, portion of drain region), as annotated in *Ryu*'s Figure 2A below. *See* EX1003, ¶53. EX1002, ¶98.



EX1003, FIG. 2A (annotated)

Both *Ryu* and *Williams* prevent the parasitic BJT from activating by shorting the source to the body, via p+ diffusion, using a source electrode. EX1003, Figure 2A (illustrating **source contacts 30** shorting **n+ regions 24** to p-wells 20 via **p+ regions 22**); *see, e.g.*, EX1004, Figure 15D, 15:6–8 ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together."). *See also* Section VI.D above. At least because *Ryu* and *Williams* share the common problem preventing the parasitic BJT from activating, and solve that problem in the same way, *i.e.*, by shorting the body to the

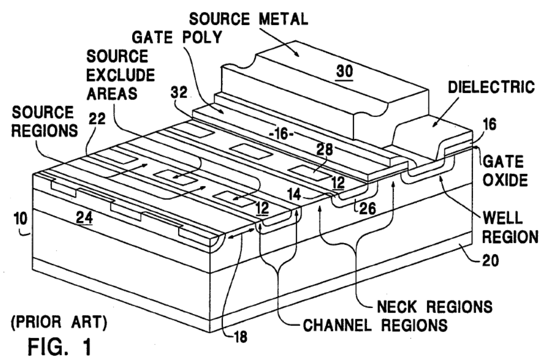
source, a POSITA would have recognized that features of *Williams*, such as *Williams*'s well-known linear geometry, were applicable in *Ryu*. EX1002, ¶99.

Furthermore, although *Ryu* is directed to silicon-carbide MOSFETS and *Williams* to silicon MOSFETs, *Baliga* teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:22–38. *Ghezzo* also teaches a method of replacing the conventional double-diffusion used in silicon MOSFETs with a double ion implantation sequence for SiC MOSFETs. EX1021, 1:56–63. EX1002, ¶100.

Accordingly, a POSITA would have understood that the teachings of *Williams* were directly applicable to *Ryu*'s SiC MOSFETs. *Id.*, ¶101.

Implementing *Ryu*'s MOSFET in a linear cell structure such that *Ryu*'s **n+ regions 24** and, consequently, *Ryu*'s **source contacts 30** define and extend along a longitudinal axis as taught by *Williams* would have yielded expected, predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007); M.P.E.P. 2143(I)(A). *Ryu* discloses that "one or more **source contacts 30**, in some embodiments are formed of nickel (Ni), titanium (Ti), platinum (Pt) or aluminum (Al), combinations thereof . . . to provide an ohmic contact to both the p+ regions 22 and the **n+ regions 24**." EX1003, ¶47. *Ryu*'s **source contacts 30** are formed from a conductor in physical contact with the **n+ regions 24**. As described above,

Williams teaches, in Figure 19E, for example, an **N+ source region** that extends along a longitudinal axis. As also described above, the linear cell arrangement of *Williams* was well-known in the art, as shown by, for example, *Rexer* (at left, below) and Baliga (at right, below), and as explained above, would have been an obvious design choice for *Ryu*'s cell structure having predictable results. EX1002, ¶102.



EX1015, FIG. 1

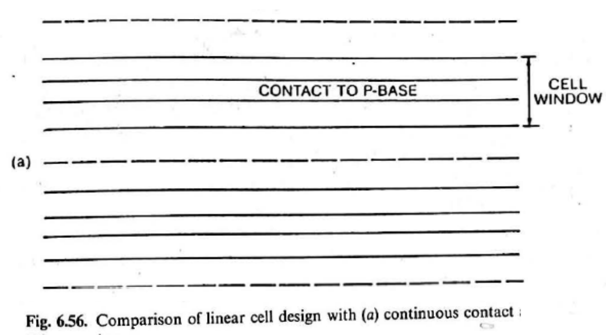


Fig. 6.56. Comparison of linear cell design with (a) continuous contact

EX1016, FIG. 6.56(a)

A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because forming *Ryu*'s structure using *Williams*'s linear cell arrangement would have been obvious to try. *KSR,* 550 U.S., 421; M.P.E.P. 2143(I)(E). As explained above, MOSFETs may have cross sections that are the same as or similar to the example shown in *Ryu*'s Figure 2A, yet have different—though all well-known—three-dimensional cellular structures. *See* EX1016, 338–339 ("the DMOS structure allows any conceivable cell topology as long as it meets all technological constraints such as alignment tolerances"); *id.*, Figures 6.55 and 6.56; EX1019, 15–17, 70–73, 455–457, Figures 1.13 and 3.9. Such cellular structures may include shapes that are hexagonal, square, circular, linear, or

triangular. A POSITA could have pursued any of these potential cellular structures, in particular the linear cellular structure, with a reasonable expectation of success because the analysis would have simply involved trying each one of these solutions. *See, e.g., CRFD Research, Inc. v. Matal*, 876 F.3d 1330, 1347 (Fed. Cir. 2017) ("[A] person of ordinary skill would have two predictable choices … providing [the] person of ordinary skill with a simple design choice" of choosing one solution or the other); EX1019, 455 ("[O]ne manufacturer advocates the use of a linear metal gate structure … for producing inexpensive high-voltage devices."). Moreover, this implementation of *Ryu* using a linear cellular structure would have been well within the knowledge and skillset of a POSITA. EX1002, ¶103.

iv. Reasonable Expectation of Success in Combining Ryu and Williams

A POSITA would also have had a reasonable expectation of success. The combination of *Ryu* and *Williams* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a POSITA would have been familiar with and been able to implement. The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ryu* and *Williams* are directed to vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1; EX1004, Abstract, 1:7–8, Figure 1. As discussed above, linear cell geometry was

well known and a POSITA would have expected a linear cell implementation of *Ryu*'s structure to operate, just as linear cell implementations of other MOSFETs were known to operate. A POSITA would have had a reasonable expectation of success in implementing *Ryu*'s MOSFET in a linear geometry because *Ryu*'s underlying specification was designed to be extensible and flexible in its application to well-known cellular shapes and layouts. EX1003, ¶¶38 ("This invention may, however, be embodied in many different forms…"), 63, 66. EX1002, ¶104.

Accordingly, *Ryu* in view of *Williams* renders obvious element 9[d] and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success. EX1002, ¶105.

f) 9[e]: "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;"

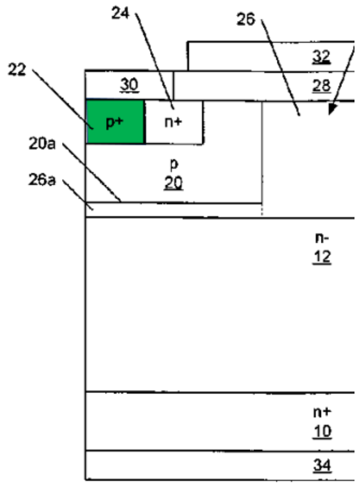
The combination of *Ryu* and *Williams* renders element 9[e] obvious. As explained below, *Ryu*'s **p+ regions 22** are base contact regions. Moreover, it would have been obvious to form a plurality of *Ryu*'s **p+ regions 22** in the **n+ source regions 24** described in limitation 9[c], above, and spaced apart from each other in a direction parallel to the longitudinal axis defined by the **source contact 30**, all as taught by *Williams*. A POSITA would have been motivated to make this

combination for the reasons discussed below and would have had a reasonable expectation of success in doing so. EX1002, ¶106.

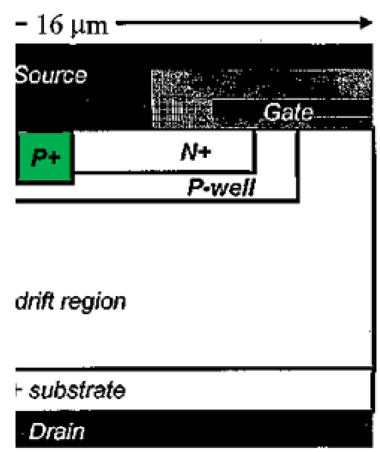
i. "base contact region"

Ryu discloses that "**regions of n+ silicon carbide 24** and . . . **regions of p+ silicon carbide 22** are disposed within p-wells 20" and that the "**regions of p+ silicon carbide 22** may be adjacent the **regions of n+ silicon carbide 24**." EX1003, ¶45. A POSITA would have understood that *Ryu*'s **p+ regions 22** are base contact regions because *Ryu*'s **p+ regions 22**: (1) correspond to the same "p+ contacts" in *Ryu*'s other articles describing the same structure; and (2) provide low resistance ohmic contact to the p-wells 20 to short the source to the base as was well known in the art. EX1002, ¶107.

First, the **p+ regions 22** in *Ryu*'s Figure 2A correspond to the P+ regions in double-implanted MOSFETs that the inventor of *Ryu* illustrates in prior and contemporaneous articles. *See* EX1023, Figure 1 (annotated along with *Ryu*'s Figure 2A to show the P+ regions in green); EX1024, Figure 2. EX1002, ¶108.



EX1003, FIG. 2A
(excerpted annotated)



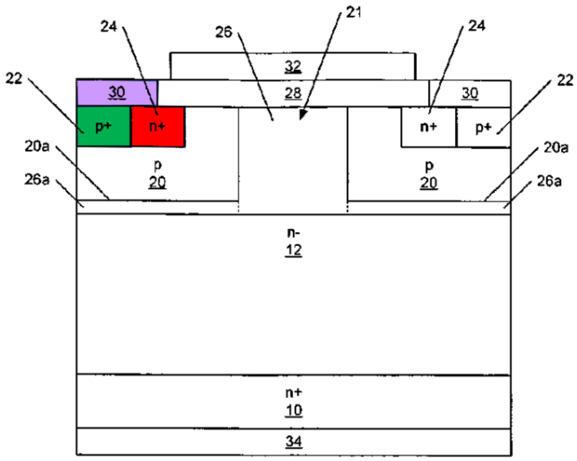
EX1023, FIG. 1
(excerpted and annotated)

These P+ regions are explicitly disclosed to be "p$^+$ contacts to the p-wells." EX1023, 321 ("A heavy dose aluminum implantation formed ***p$^+$* contacts to the p-wells**,…"); EX1024, 881 (describing the same "***p$^+$* contacts to the p-wells**"). Like the p+ region in Ryu's articles, a POSITA would have understood *Ryu*'s **p+ regions 22** provide contacts to the p-wells 20. EX1002, ¶109.

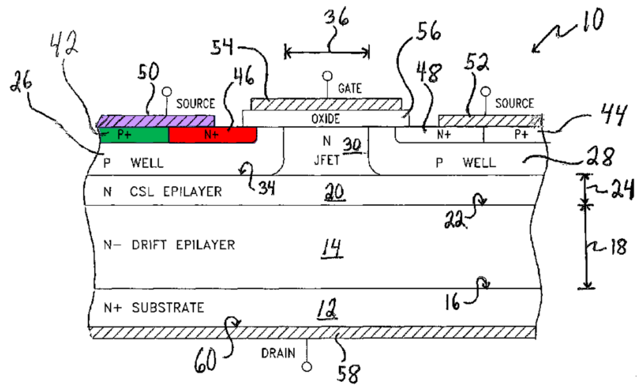
Second, a POSITA would have understood that *Ryu*'s **p+ regions 22** provide low resistance ohmic contact to the p-wells 20. *See* Section VI.D above. As *Ghezzo* explains, "[a]lthough an electrical connection can be made directly to the p type base region, the p+ ***base contact region*** provides an improved connection." EX1021, 5:28–30; *see also* EX1004, 6:24–26 ("the integration of a shallow P+ region used to achieve a low resistance ohmic contact to the body"); *id.*, 16:32–34 ("maximize the ***P+ contact to the body region*** (to suppress parasitic bipolar turn-on, prevent

snapback and ruggedize the device)"); EX1006, 5:59–64 ("The base regions 11 . . . can be doped more heavily by additional implantation of aluminum for a higher latch-up strength . . . in the ***base contact region*** 12 at the source electrode 15, and thus be p+-conducting."). As exemplified by *Ghezzo*, a POSITA would have understood that *Ryu's* p+ region provides the desired low resistance connection to the base, and is therefore a "base contact region." EX1002, ¶110.

Additionally *Ryu*'s Figure 2A and the '633 patent's Figure 1 are reproduced below. As shown, *Ryu*'s **p+ regions 22** and the '633 patent's "base contact regions" 42 and 44 are both p+ regions that are disposed between the source contact (30 for *Ryu* and 50 for the '633 patent) and the P well (20 for *Ryu* and 26 for the '633 patent). *Ryu*'s **p+ regions 22** have the same doping with p-type impurities as the "base contact regions" 42 and 44 of the '633 patent. *Cf.* EX1003, ¶¶45, 55 ("…p-type impurities are implanted utilizing the mask 106 to provide the **p+ regions 22**.") EX1001, 6:66–7:2 ("The base electrode regions 42, 44 are doped with P-type impurities to a 'P+' concentration.") Moreover, *Ryu*'s **p+ regions 22** perform the same function as the '633 patent's "base contact regions" 42 and 44, *i.e.*, both provide low resistance between the source contact and the P well. For these reasons, both are "base contact regions." EX1002, ¶111.



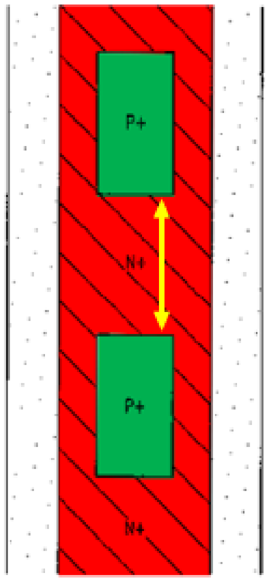
EX1003, FIG. 2A (annotated)



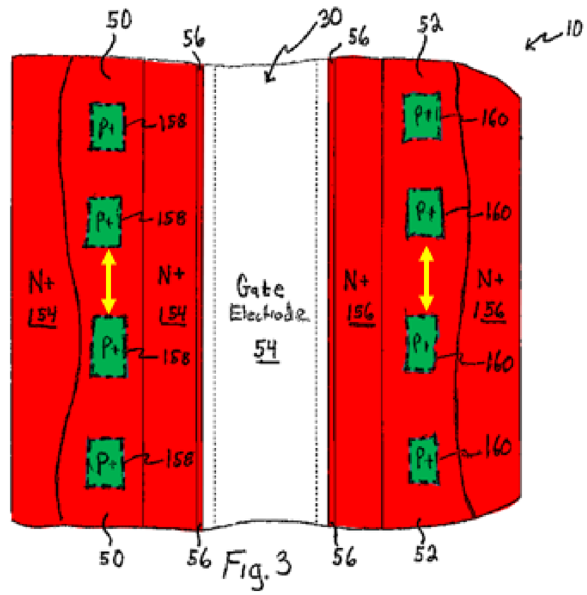
EX1001, FIG. 1 (annotated)

ii. "a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode"

Ryu does not explicitly disclose a plurality of left **p+ regions 22** defined in the left **n+ region 24** and spaced apart from each other in a direction parallel to the longitudinal axis defined by the left **source contact 30**. However, *Williams* does. Specifically, *Williams* discloses "a continuous **N+ source region** with **P+ body contact** 'windows'" in Figure 19E (reproduced below, alongside the '633 patent's Figure 3 for comparison). EX1004, 10:23–24. As shown in *Williams*'s Figure 19E, the **P+ body contact** windows are "*defined in*" the **N+ source region** and are "*spaced apart from each other in the direction of a longitudinal axis*" (*i.e.*, up-down with respect to the page), as annotated using yellow arrows, in just the same way as shown in the '633 patent. It would have been obvious to use *Williams*'s configuration of **P+ body contacts** in *Ryu*. EX1002, ¶112.



EX1004, FIG. 19E (annotated)



EX1001, FIG. 3 (annotated)

A POSITA would have understood that a source electrode (*e.g.*, a metal or other conductive layer, such as *Ryu*'s **source contacts 30**) would be laid in the direction of the longitudinal axis on top of and make electrical contact to both the **P+ body contact** windows and the **N+ source region**. *See* EX1004, 15:6–8, Figure 15D ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together."). EX1002, ¶113.

Thus, when implemented with *Williams*'s topology, *Ryu*'s **p+ regions 22** would be defined in the **N+ source region** and spaced apart from each other in a direction parallel to the longitudinal axis defined by the source electrode just as *Williams*'s **P+ body contact** windows are positioned. *Id.*, ¶114.

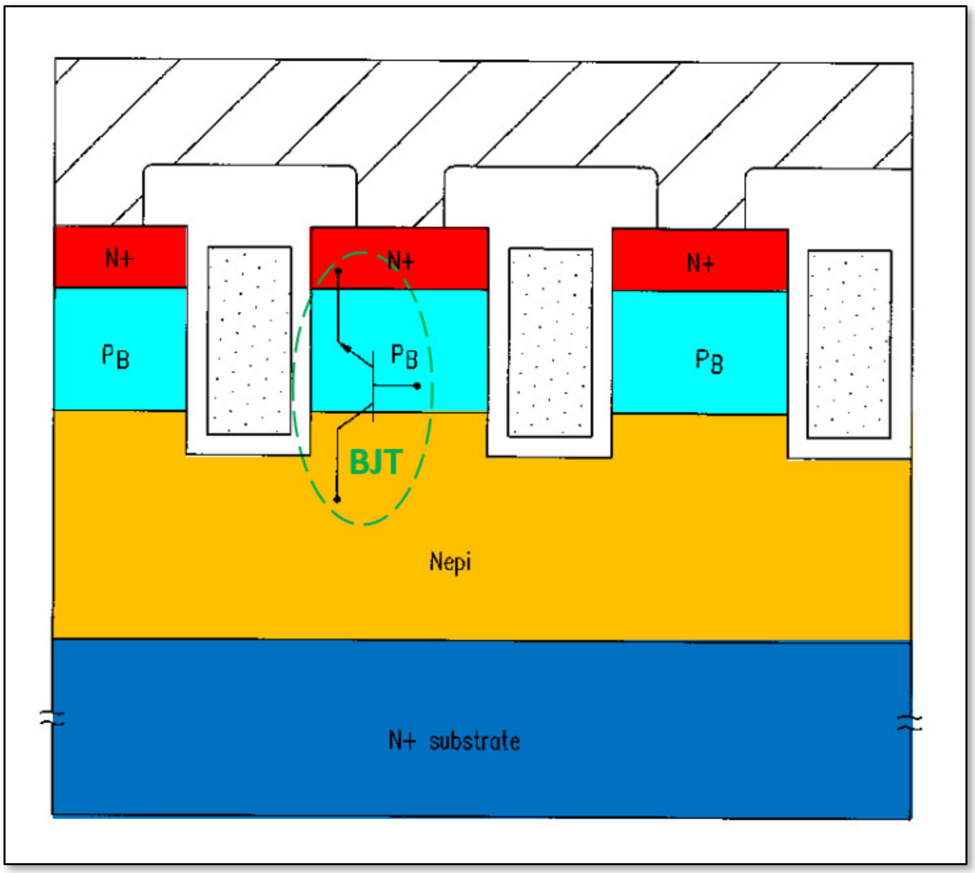
iii. Motivation to Combine Ryu and Williams

A POSITA would have been motivated to modify *Ryu*'s MOSFET according to and informed by *Williams*'s teachings such that *Ryu*'s left **p+ region 22** is defined repeatedly in the left **n+ region 24**, and the repeated left **p+ regions 22** are spaced apart from each other in a direction parallel to the longitudinal axis defined by the left **source contact 30**. EX1002, ¶115.

Ryu and *Williams* are from the same field of endeavor. *See, e.g.*, *Medtronic*, 721 F.2d, 1574–75; M.P.E.P. § 2141. Both references are directed to vertical MOSFETs. *Ryu* discloses embodiments of vertical MOSFETs that "may reduce on-state resistance" compared to conventional vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1. *Williams* discloses structures for vertical MOSFETs that are used to reduce on-resistance. *See, e.g.*, EX1004, Figure 1, 8:15–16 ("reduce the on-resistance of the DMOSFET"), 16:31–32 ("achieve the lowest possible resistance"). Thus, both references are directed to vertical MOSFETs and aim at reducing on-resistance. EX1003, ¶6; EX1004, 1:7–8. EX1002, ¶116.

Although *Williams* discloses MOSFETs with trench gates and *Ryu* discloses planar gates, a POSITA would nonetheless have been motivated to use *Williams*'s teachings in *Ryu*. This is because *Williams*'s and *Ryu*'s MOSFETs share many common features to which the shape of the gate is irrelevant. For example, both *Williams*'s trench-gated vertical MOSFETs and *Ryu*'s non-trench-gated vertical

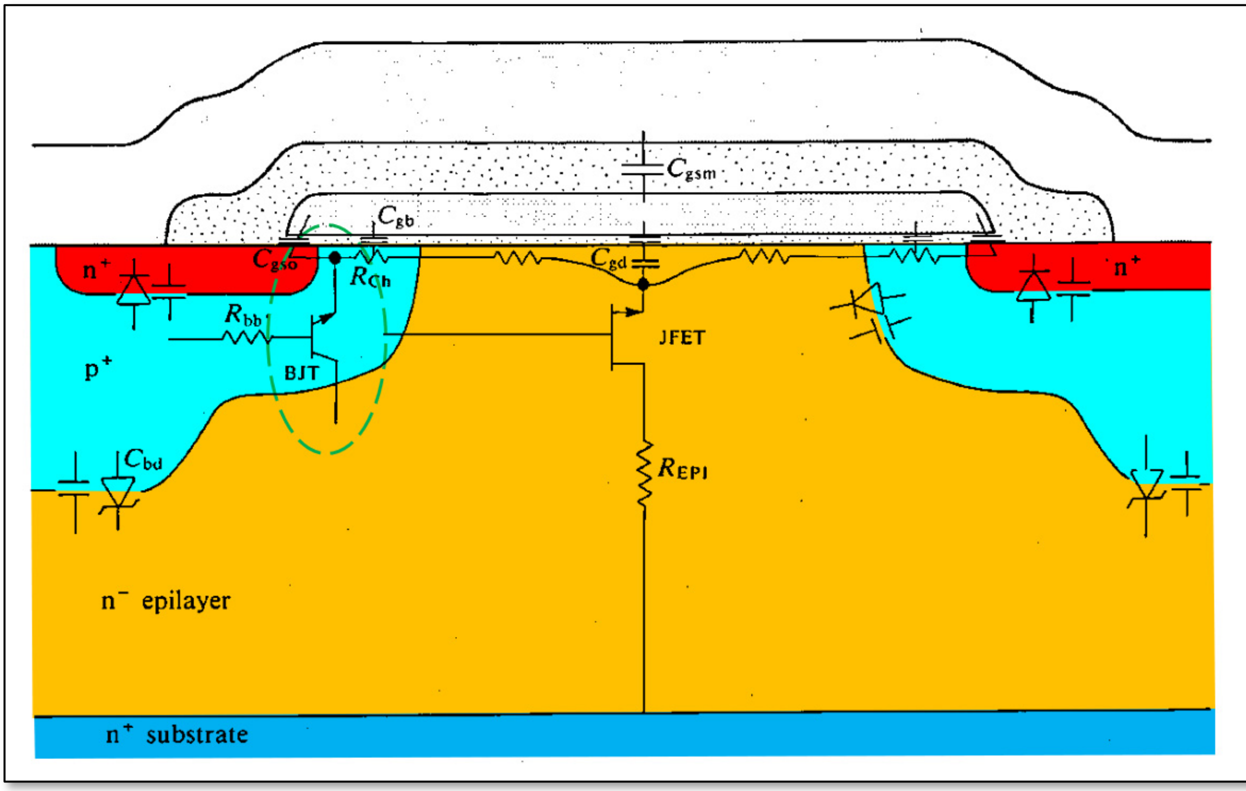
MOSFET include a parasitic BJT within the epilayer that could inadvertently be activated. For both *Williams* and *Ryu*, the solution to the problem caused by this parasitic transistor is the same. For example, *Williams* describes such a "parasitic NPN bipolar transistor," which it illustrates in Figure 7A (reproduced below). EX1004, 6:9. EX1002, ¶117.



EX1004, FIG. 7A (annotated)

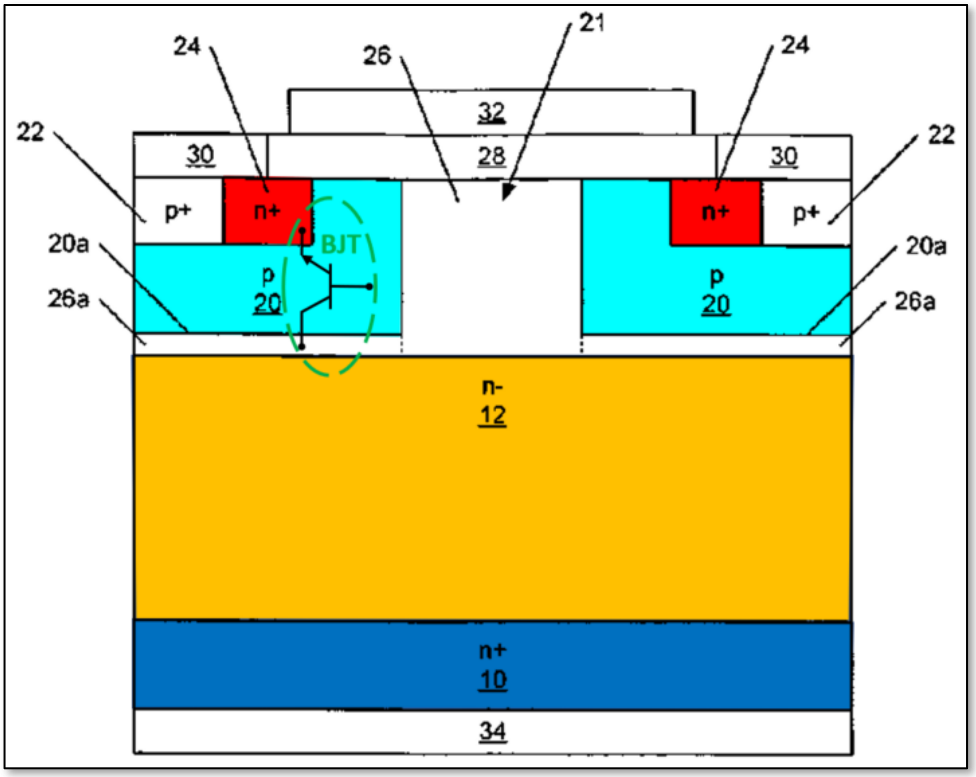
Williams's parasitic BJT is formed between the source, the body, and the drain in the same way *Grant* illustrates a parasitic BJT formed between the source, the

body, and the drain of a non-trench-gated vertical MOSFET in Figure 3.15, reproduced below. EX1002, ¶118.



EX1019, Figure 3.15 (annotated)

Based on at least *Grant*'s teachings, a POSITA would have understood that a parasitic npn BJT would also be formed in *Ryu*'s MOSFET between the n+ region 24 (*i.e.*, source region), p-well 20 (*i.e.*, body), and the n-type epitaxial layer 26 (*i.e.*, portion of drain region), as annotated in *Ryu*'s Figure 2A below. *See* EX1003, ¶53. EX1002, ¶119.



EX1003, FIG. 2A (annotated)

Both *Ryu* and *Williams* prevent activation of the parasitic BJT by shorting the source to the body, via p+ diffusion, using a source electrode. EX1003, Figure 2A (illustrating **source contacts 30** shorting **n+ regions 24** to p-wells 20 via **p+ regions 22**); *see, e.g.*, EX1004, Figure 15D, 15:6–8 ("Metal layer [158] contacts both N+ source region 159 and P+ body contact region 160, thereby shorting the source and body together."). *See also* Section VI.D above. *Williams* further discloses "various source-body designs" in Figures 19A–19F and the need to maximize the contact of the **P+ body contact regions** to the body region to "suppress parasitic bipolar turn-on, prevent snapback and ruggedize the device." EX1004, 10:17–18; 16:32–33. A

POSITA would have recognized the advantages of using a plurality of **P+ body contact regions** as taught by *Williams*. Lithographically, it has been standard practice to use multiple contact regions rather than one larger contact region, since this simplifies lithographic control and etch uniformity during the fabrication process. As such, when using a longitudinally rectangular structure, disposing a plurality of contact regions on it would have been readily known and obvious to a POSITA; indeed, this has been the most common approach used in the industry. Therefore, a POSITA would have been motivated to use *Williams*'s teachings of multiple and periodic **P+ body contact regions** in *Ryu* to maximize the contact of the p+ regions and ruggedize *Ryu*'s MOSFET. EX1002, ¶120.

Furthermore, although *Ryu* is directed to silicon-carbide MOSFETS and *Williams* to silicon MOSFETs, *Baliga* teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." EX1005, 4:22–38. *Ghezzo* also teaches a method of replacing the conventional double-diffusion used in silicon MOSFETs with a double ion implantation sequence for SiC MOSFETs. EX1021, 1:56–63. EX1002, ¶121.

Accordingly, a POSITA would have understood that the teachings of *Williams* were directly applicable to *Ryu*'s SiC MOSFETs. *Id.*, ¶122.

Implementing *Ryu*'s MOSFET such that *Ryu*'s left **p+ region 22** are defined repeatedly in the left **n+ region 24** as taught by *Williams* would have yielded expected, predictable results. *KSR*, 550 U.S., 416; M.P.E.P. 2143(I)(A). *Ryu* discloses adjacent left **p+ region 22** and left **n+ region 24** disposed within the p-well 20 on the left. EX1003, ¶45, Figure 2A. *Williams* also discloses adjacent N+ source region 12 and a P+ body contact region 13. EX1004, 1:9–10, Figure 1. Additionally, *Williams* discloses a continuous **N+ source region** with **P+ body contact** windows. *Id.*, 10:23–24, Figure 19E. A POSITA would have been motivated to combine the elements taught by *Ryu* and *Williams*—namely, the left **p+ region 22** and left **n+ region 24** as taught by *Ryu*, and the continuous **N+ source region** with **P+ body contact** windows as taught by *Williams*—using known and routine semiconductor fabrication techniques to modify the shape and location of *Ryu*'s left **p+ region 22** and left **n+ region 24** such that the left **p+ region 22** is defined repeatedly in the left **n+ regions 24** because, as *Williams* teaches, such a configuration would help reduce on-resistance, while continuing to provide the needed connection between the **n+ regions 24** and the p-wells 20 via the **p+ regions 22** to ruggedize *Ryu*'s MOSFET against unwanted activation of the parasitic BJT. EX1004, 17:18 ("better N+ contact resistance"); *id,* 6:8–9 ("The source-to-body short prevents conduction and snapback breakdown of the parasitic NPN bipolar transistor . . ."). This result would have been readily predictable and recognized by

a POSITA because, as *Williams* points out, it was well-known that "[t]he primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents." A POSITA would have been motivated to modify *Ryu*'s p+ regions according to the teachings of *Williams* so as to achieve the lower on-resistance, while maintaining the connection between *Ryu*'s **n+ regions 24** and p-wells 20 via the **p+ regions 22**. EX1004, 1:33–37. As discussed above in Section VI.C, a lower on-resistance minimizes voltage drop and power dissipation (*i.e.*, power loss), and maximizes the current rating of the MOSFET. *See* EX1019, 18, 74–75. And as discussed in Section VI.D, connecting the source to the body through p+ regions ruggedizes a MOSFET against unwanted turn on of the parasitic BJT. *See, e.g.*, *id.*, 90, Figure 1.11. EX1002, ¶123.

A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because it would have been a simple substitution of one known element (adjacent left **p+ region 22** and left **n+ region 24** in *Ryu*) for another (continuous **N+ source region** with **P+ body contact** windows as taught by *Williams*) to obtain predictable results. *KSR*, 550 U.S., 416; M.P.E.P. 2143(I)(B). This substitution would have been readily achievable by a POSITA via known and routine semiconductor fabrication techniques to form *Ryu*'s adjacent left **p+ region**

22 and left **n+ region 24** into a continuous **n+ region 24** with windows of **p+ region 22**. EX1002, ¶124.

A POSITA would have been further motivated to combine the teachings of *Ryu* and *Williams* because forming *Ryu*'s adjacent left **p+ region 22** and left **n+ region 24** into a continuous **n+ region 24** with windows of **p+ region 22** would have been obvious to try. *KSR,* 550 U.S., 421; M.P.E.P. 2143(I)I. As *Williams* illustrates in Figures 19A–19F, there were numerous (at least six) known and predictable choices for forming adjacent **N+** and **P+** regions. A POSITA could have pursued these potential solutions with a reasonable expectation of success because the analysis would have simply involved trying each one of these solutions. *See, e.g., CRFD Research*, 876 F.3d, 1347 ("[A] person of ordinary skill would have two predictable choices … providing [the] person of ordinary skill with a simple design choice" of choosing one solution or the other). Thus, it would have been obvious to a POSITA to have formed *Ryu*'s left **p+ region 22** and left **n+ region 24** into a continuous **n+ region 24** with windows of **p+ region 22**, as *Williams* teaches in Figure 19E. EX1002, ¶125.

The modification of *Ryu*'s left **p+ region 22** and left **n+ region 24** to be in the form of *Williams*'s continuous **N+ source region** with **P+ body contact** windows would have been readily implemented by simply modifying the masks used to form *Ryu*'s left **p+ region 22** and left **n+ region 24**. A POSITA could have implemented

this modification using basic semiconductor fabrication techniques to modify *Ryu*'s masks such that *Ryu*'s left **p+ region 22** and left **n+ region 24** are formed as a continuous **n+ region 24** with windows of **p+ region 22** as taught by *Williams*. EX1002, ¶126. This modification would have been well within the knowledge and skillset of a POSITA. Indeed, the '633 patent implicitly confirms this. When the '633 patent discusses the different geometric shapes for the N+/P+ regions in Figures 2, 3 and 4, there is no discussion of special manufacturing steps required, but only the advantages and disadvantages of the shapes themselves. *Id*.

iv. Reasonable Expectation of Success in Combining Ryu and Williams

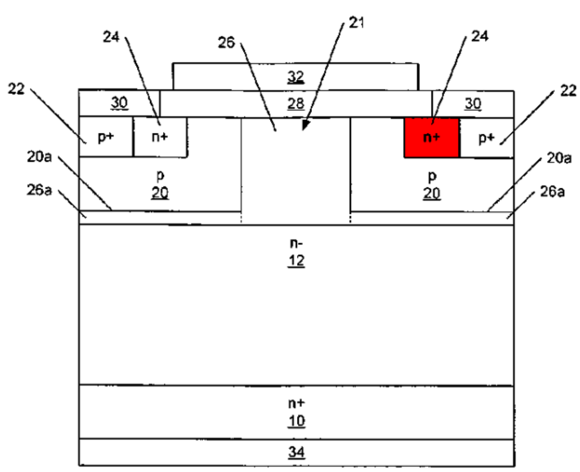
A POSITA would also have had a reasonable expectation of success. The combination of *Ryu* and *Williams* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a POSITA would have been familiar with and been able to implement, and which *Williams* explains how to accomplish. EX1004, 29:1–19 ("P+ Body Contact Formation"). The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ryu* and *Williams* are directed to vertical MOSFETs. EX1003, ¶¶6, 9, 39, Figure 1; EX1004, Abstract, 1:7–8, Figure 1. A POSITA would have had a reasonable expectation of success in modifying *Ryu*'s MOSFET because

Ryu's underlying specification was designed to be extensible and flexible. EX1003, ¶¶38 ("This invention may, however, be embodied in many different forms…"), 63, 66. Such modifications were expected to be performed when optimizing the on-resistance and ruggedness of power MOSFETs. *See, e.g.*, EX1004, 16:28–17:19. EX1002, ¶127.

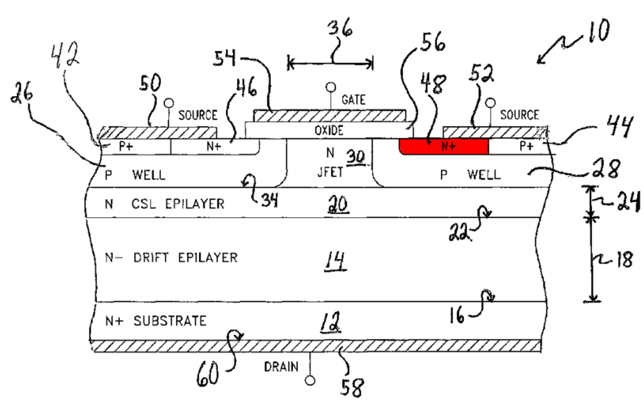
Accordingly, *Ryu* in view of *Williams* renders obvious element 9[e] and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success. EX1002, ¶128.

g) 9[f]: "a second source region;"

Ryu discloses element 9[f]. As discussed above with respect to element 9[c], *Ryu*'s **n+ regions 24** correspond to the '633 patent's **source regions 46 and 48**. Thus, *Ryu* discloses at least a first n+ region 24 (*i.e., "a first source region*") on the left and a second **n+ region 24** (*i.e.*, "*a second source region*") on the right, for example, as shown in the annotated figures below. EX1002, ¶129.



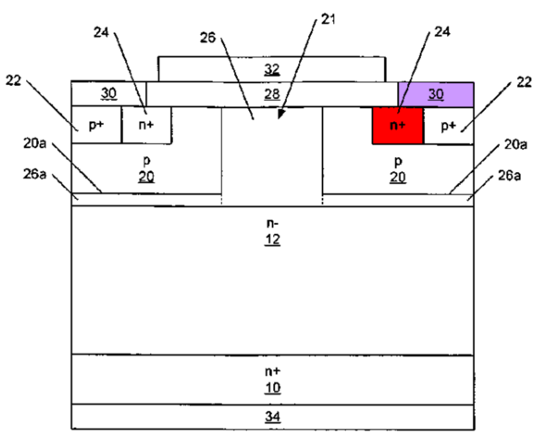
EX1003, FIG. 2A (annotated)



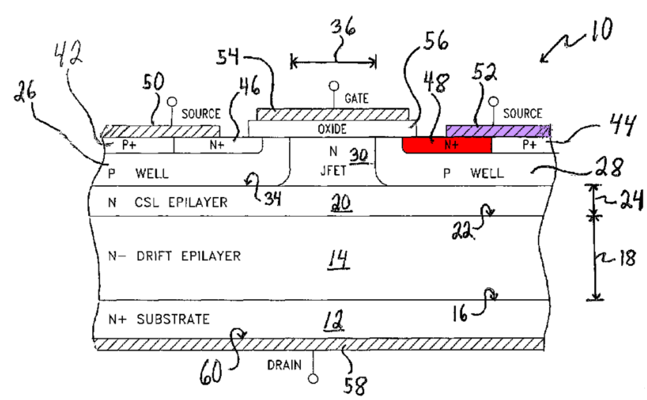
EX1001, FIG. 1 (annotated)

h) 9[g]: "a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;"

The combination of *Ryu* and *Williams* renders element 9[g] obvious. For the same reasons described for element 9[d], *Ryu* discloses, with respect to Figure 2A (reproduced below, alongside the '633 patent's Figure 1) for example, a second **source contact 30** (*i.e.*, "*a second source electrode*") on the right formed over the right **n+ region 24** (*i.e.*, "*the second source region*"). As further described for element 9[d], a POSITA would have understood that, if fabricated as a linear cell, *Ryu*'s cross-sectional view of its MOSFET would extend perpendicularly to the page, and, therefore, the second **source contact 30** would likewise define a longitudinal axis perpendicular to the page. Also, for the same reasons described for elements 9[d] and 9[e], a POSITA would have found it obvious to implement *Ryu*'s MOSFET using a linear geometry such that the **source contact 30** defines a longitudinal axis. EX1002, ¶130.



EX1003, FIG. 2A (annotated)



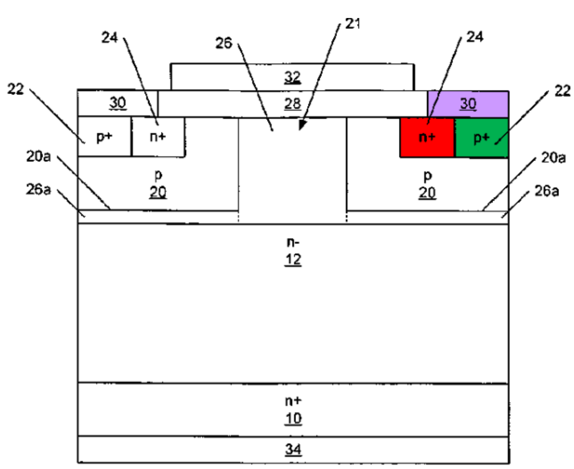
EX1001, FIG. 1 (annotated)

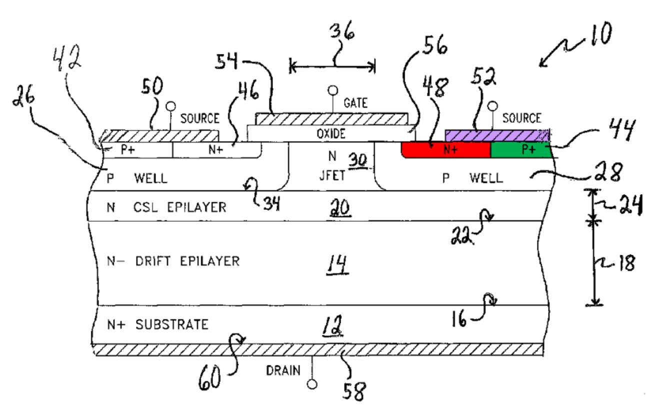
i) 9[h]: "a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and"

For the same reasons described with respect to element 9[e], the combination of *Ryu* and *Williams* renders element 9[h] obvious. EX1002, ¶131.

i. "base contact region"

As discussed above with respect to element 9[e], *Ryu*'s **p+ regions 22** correspond to the '633 patent's base contact regions 42 and 44, and the left **p+ region 22** corresponds to a first base contact region. Thus, *Ryu*'s second/right **p+ region 22**, which is adjacent to the right **n+ region 24** (*i.e.*, "*the second source region*"), corresponds to a second base contact region. EX1002, ¶132. As also discussed above, a POSITA would have understood that the right **source contact 30** (*i.e.*, "*the second source electrode*") defines a longitudinal axis perpendicular to the page. *Id.*, ¶132.





EX1003, FIG. 2A (annotated) | EX1001, FIG. 1 (annotated)

ii. "a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode"

Ryu does not explicitly disclose a plurality of right **p+ regions 22** defined in the right **n+ region 24** and spaced apart from each other in a direction parallel to the longitudinal axis defined by the right **source contact 30**. However, as discussed above with respect to element 9[e], *Williams* discloses "a continuous **N+ source region** with **P+ body contact** 'windows'" in Figure 19E. EX1004, 10:23–24. Using the same rationale as in Sections X.A.1.f.iii and iv, a POSITA would have been motivated to modify *Ryu* in view of *Williams* such that *Ryu*'s right **p+ region 22** is defined repeatedly in the right **n+ region 24**, and the repeated **p+ regions 22** are spaced apart from each other in a direction parallel to the longitudinal axis defined by the right **source contact 30**, and would have had a reasonable expectation of success in doing so. EX1002, ¶133.

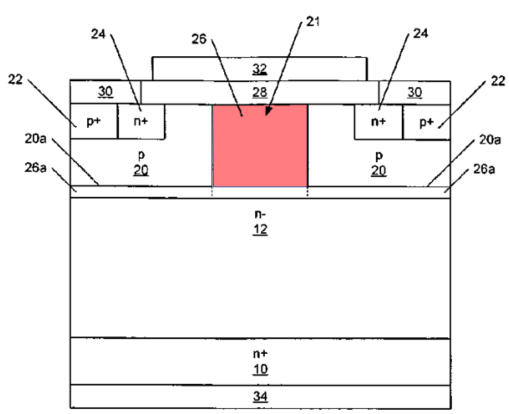
Accordingly, *Ryu* in view of *Williams* renders obvious element 9[h]. *Id.*, ¶134.

j) 9[i]: "a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers."

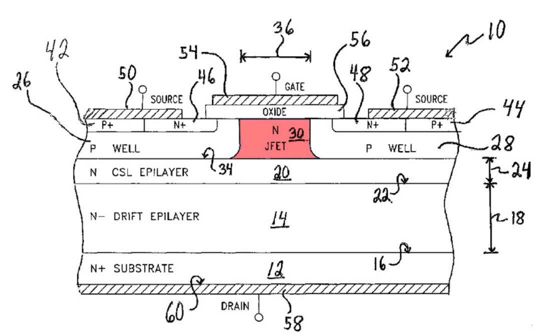
Ryu discloses element 9[i]. As explained below, *Ryu* expressly discloses a "*JFET region.*" *Ryu*'s "JFET region" is defined between the first and second source regions in the same way as in the '633 patent. Moreover, *Ryu*'s "JFET region" is disclosed as having a range of width that substantially overlaps with the range of "*less than about three micrometers*." EX1002, ¶135.

i. "a JFET region"

Ryu expressly discloses that the gap between the p-wells 20 "may be referred to as the **JFET region 21**." EX1003, ¶44; *cf.* EX1001, 6:3–5 ("The remaining region of the additional epitaxial layer between the wells 26, 28 forms the JFET region 30."). *Ryu*'s **JFET region 21** in Figure 2A is shown beside the '633 patent's "JFET region" below, both annotated in salmon. EX1002, ¶136.



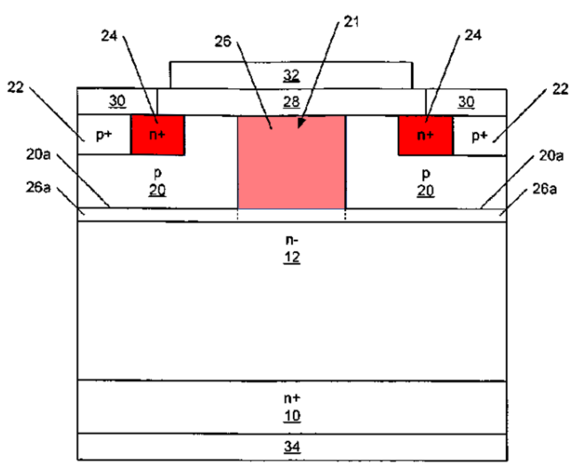
EX1003, FIG. 2A (annotated)



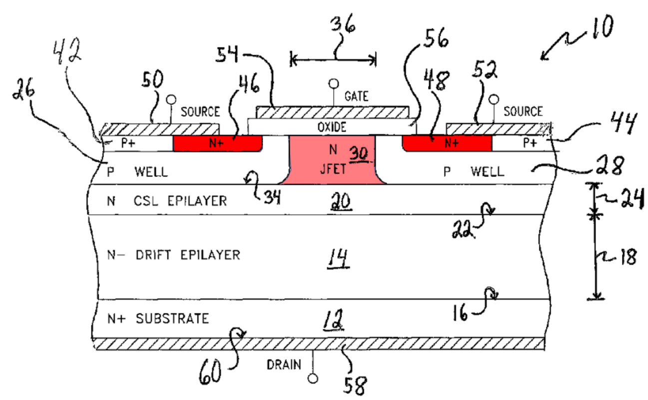
EX1001, FIG. 1 (annotated)

ii. "defined between the first source region and the second source region"

Ryu's **n+ regions 24** (*i.e.*, the "*first source region*" and "*second source region*") are disposed within p-wells 20. And *Ryu* states that "the region [between the p-wells 20] may be referred to as the JFET region 21." EX1003, ¶44. The **JFET region 21** is as illustrated in Figure 2A, for example. As such, *Ryu* discloses that the **JFET region 21** is between the first and second source regions. Also, as shown below, *Ryu*'s arrangement is identical to that shown in the '633 patent, where both structures include a portion of each p-well between the JFET region and each source region disposed within each respective p-well. Accordingly, *Ryu*'s **JFET region 21** is "*defined between the first source region and the second source region*" in the same way as the '633 patent's JFET region. EX1002, ¶137.



EX1003, FIG. 2A (annotated)



EX1001, FIG. 1 (annotated)

iii. "the JFET region having a width less than about three micrometers"

Ryu discloses that "if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region 21** may become very high," and thus "gaps of from about 1 µm to about 10 µm are preferred." EX1003, ¶44. Thus, *Ryu* discloses that the **JFET region 21** may have a width of less than about three micrometers because the recited width of "less than about three micrometers" is disclosed with sufficient specificity by *Ryu*'s disclosure of a JFET width "from about 1 [micrometer] to about 10 [micrometers]." EX1002, ¶138. *See also ClearValue Inc. v. Pearl River Polymers Inc.*, 668 F.3d 1340, 1345, 101 USPQ2d 1773, 1777 (Fed. Cir. 2012) (finding a claimed narrow range was disclosed with "sufficient specificity" by a reference disclosing a broader range where, like here, there was "no 'considerable difference between the claimed range and the range in the prior art.'" (internal citations omitted)).

Therefore, *Ryu* in view of *Williams* renders claim 9 obvious. *Id.*, ¶139.

2. Dependent Claim 10

"The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a width of about one micrometer."

Ryu in view of *Williams* renders obvious claim 9, as discussed above. *Ryu* discloses the additional limitation of claim 10. For example, *Ryu* discloses that "if the gap [between the p-wells 20] is too narrow, the resistance of the **JFET region**

21 may become very high," and thus "gaps of from about 1 µm to about 10 µm are preferred." EX1003, ¶44; *see also ClearValue*, 668 F.3d, 1345. Therefore, *Ryu* discloses the **JFET region 21** may have a width of about one micrometer. EX1002, ¶140.

Thus, *Ryu* in view of *Williams* renders claim 10 obvious. *Id.*, ¶141.

3. Dependent Claim 11

> ***"The double-implanted metal-oxide semiconductor field-effect transistor of claim 9, wherein the JFET region has a first concentration of first type impurities and the drift semiconductor layer has a second concentration of first type impurities, the first concentration of first type impurities being greater than the second concentration of first type impurities."***

Ryu in view of *Williams* renders obvious claim 9, as discussed above. *Ryu* discloses the additional limitation of claim 11. For example, *Ryu* expressly discloses that "the gap 21 [(*i.e.*, the **JFET region 21**)] between the p-wells 20 has a higher carrier concentration than the drift layer 12." EX1003, ¶42. Indeed, because the **JFET region 21** is the gap that remains in region 26 after the p-wells 20 are formed, the **JFET region 21** has the dopant type and concentration of region 26—n-type impurities (*i.e.*, "*first type impurities*") at a concentration of "about 10^{15} to about 5×10^{17} cm^{-3}" (*i.e.*, "*a first concentration*"). EX1003, ¶41. And the **drift layer 12** is doped to an "n–" (*i.e.*, also n-type, "*first type impurities*") concentration of "about 10^{14} to about 5×10^{16} cm^{-3}" (*i.e.*, "*a second concentration*"). *Id.*, ¶40. *Ryu* expressly

explains that "[t]he region 26 ***has a higher carrier concentration*** than the carrier concentration of the **drift layer 12** . . . " *Id.*, ¶41. Relatedly, as discussed in Section VI.C, *Grant* teaches that "[i]ncreasing the donor doping concentration in the drain throats [(*i.e.*, the JFET regions)] . . . has two beneficial effects"—"the cell size can be reduced and . . . lower $R_{DS(on)}$ can be realized." EX1019, 83–84. Thus, a POSITA would have been motivated by such a teaching to make the doping concentration of the JFET region greater than that of the drift region in the epilayer. Accordingly, because *Ryu*'s **JFET region 21** can have a "*first concentration*" that is an order of magnitude, or more, greater than the "*second concentration*" of **drift layer 12**, *Ryu* discloses "*the first concentration of first type impurities being greater than the second concentration of first type impurities.*" EX1002, ¶142.

***Ryu* structure**	**Concentration (cm^{-3})**	**EX1003 cite**
JFET region 21	About 10^{15} to about 5×10^{17} ("*first concentration*")	¶41
Drift layer 12	About 10^{14} to about 5×10^{16} ("*second concentration*")	¶40

Thus, *Ryu* in view of *Williams* renders claim 11 obvious. EX1002, ¶143.

XI. CO-PENDING DISTRICT COURT LITIGATION IN TEXAS SHOULD NOT PRECLUDE INSTITUTION

Although there is concurrent district court litigation involving the ’633 patent, the weight of the factors described in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5-6 (PTAB Mar. 20, 2020) (precedential) favors institution of this Petition.

A. The potential for a stay of the district court case urges against denial (factor 1)

After any institution of review based on this Petition, ST intends to seek a stay of the co-pending district court proceedings. Therefore, factor 1 is neutral because any decision by the district court to stay the case would issue after institution and be based on “a variety of circumstances and facts beyond [the Board’s] control and to which the Board is not privy.” *See Sand Revolution II, LLC v. Cont’l Intermodal Grp. Trucking, LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

B. Uncertainty over the trial date in the Texas case favors institution (factor 2)

The district court recently entered a Scheduling Order identifying April 24, 2023 as the target trial date. EX1026, 5. Based on the expected 18-month IPR schedule, a final written decision (FWD) in this proceeding would likely issue by June 2023—within less than two months of the court’s initial target date for trial.

The close proximity between the district court's target trial date and the Board's FWD date favors institution, or is neutral, because the district court's trial date is subject to considerable uncertainty. *Sand Revolution*, IPR2019-01393, Paper 24 at 9-10 (uncertainty of trial date weighed in favor of institution) (informative); *Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01008, Paper 10 at 14 (PTAB Dec. 7, 2020) ("due to the uncertainty as to this trial date, this factor is, at most, neutral").

Despite the district court's aspirational target date, trial is unlikely to begin on April 24, 2023 and may be postponed until after the Board issues a FWD in this proceeding. Delays may result from (i) the continued impact of and uncertainty surrounding the COVID-19 pandemic, (ii) the court's crowded docket, which currently includes over 815 pending patent cases (EX1027), and (iii) the tendency for trial dates in the Western District of Texas to slip from the court's initial target dates—EX1028, 3 ("In the WDTX, 70% of trial dates initially relied upon by the PTAB to deny petitions have slid.").

In contrast to the potential delays to the district court's schedule, the Board's schedule is unlikely to shift. Barring exceptional circumstances, the Board must issue its FWD within the one-year statutory deadline described in 35 U.S.C. § 316(a)(11). *Sand Revolution*, IPR2019-01393, Paper 24 at 9. Further, the Board has remained fully operational despite the challenges presented by COVID-19. *Id.*

Given the circumstances, the Board may well issue a FWD before the beginning of any trial in the district court.

Factor 2 also favors institution because ST diligently filed this Petition ***seven months*** before its statutory deadline for doing so. *See, e.g.*, *Apple Inc. v.Seven Networks, LLC*, IPR2020-00156, Paper 10 at 9 & n.8 (PTAB June 15, 2020) (considering the filing date relative to potential filing dates helps to analyze factor 2 on a sliding scale based on relative trial dates).

C. Investment in the parallel district court proceeding is minimal and ST was diligent in filing this Petition (factor 3)

The co-pending district court case is still in an early phase. The court has not addressed the merits of the case. All significant stages of litigation—including discovery, claim construction, summary judgment, and trial—remain in the future. The target trial date is over 15 months away and will likely be delayed. After receiving any institution decision, ST intends to move for a stay in the district court to further minimize investment by the court and the parties. Moreover, ST was diligent in filing this Petition over ***seven months*** before its statutory bar date. *See Seven Networks*, IPR2020-00156, Paper 10 at 11 (filing petition four months before § 315(b) bar date shows diligence).

D. The Petition raises unique issues, which favors institution (factor 4)

ST expects its invalidity positions in the district court case will diverge from the ground of unpatentability described in this Petition. In any event, ST reserves the right to enter a stipulation relating to the district court case that would prevent and/or reduce overlap with the requested IPR, should the Board deem one necessary. Such a stipulation would mitigate concerns about duplicative efforts in the district court case and this IPR proceeding. *See Sand Revolution*, IPR2019-01393, Paper 24 at 12.

E. The parties overlap (factor 5)

The district court case and the IPR proceeding involve the same parties.

F. The merits of ST's challenge support institution (factor 6)

"[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record … the institution of a trial may serve the interest of overall system efficiency and integrity….". *Fintiv*, IPR2020-00019, Paper 11 at 14-15. As described above, *Ryu* and *Williams* disclose and render obvious the allegedly inventive features of the '633 patent, including the configuration recited by claim 9 and its dependents. The merits of the prior art and their close correspondence to the challenged claims favors institution.

XII. CONCLUSION

Petitioner requests institution of an IPR of the ’633 patent and cancellation of claims 9–11.

Respectfully Submitted,

Dated: December 6, 2021

/Richard Goldenberg/
Richard Goldenberg, Lead Counsel
Registration No. 38,895

TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 7,498,633
1002	Declaration of Dr. Vivek Subramanian
1003	U.S. Patent Application Publication No. 2004/0119076 ("*Ryu*")
1004	U.S. Patent No. 6,413,822 ("*Williams*")
1005	U.S. Patent No. 5,233,215 ("*Baliga*")
1006	U.S. Patent No. 6,316,791 ("*Schörner*")
1007	U.S. Patent Application No. 2006/0267092 ("*Jun*")
1008	'633 Patent File History, 4/4/2007 Non-Final Rejection
1009	'633 Patent File History, 8/6/2007 Response to Office Action
1010	'633 Patent File History, 10/12/2007 Final Rejection
1011	'633 Patent File History, 3/12/2008 Response to Office Action
1012	'633 Patent File History, 6/25/2008 Non-Final Rejection
1013	'633 Patent File History, 8/22/2008 Response to Office Action
1014	'633 Patent File History, 12/17/2008 Notice of Allowance
1015	U.S. Patent No. 5,317,184 ("*Rexer*")
1016	"Modern Power Devices," B. Jayant Baliga, 1987 (relevant sections)
1017	A. G. Jost et al., "Implementation of a VLSI Layout Tool on Personal Computers," ACM, 1990

Exhibit	Description
1018	E. S. Kuh et al., "Recent Advances in VLSI Layout," Proceedings of the IEEE, vol 78, no. 2, February 1990
1019	"Power MOSFETs – Theory and Applications," Duncan A. Grant and John Gowar, 1989 ("*Grant*") (relevant sections)
1020	J. A. Cooper, Jr. et al., "SiC Power-Switching Devices—The Second Electronics Revolution?," Proceedings of the IEEE, vol. 90, no. 6, June 2002
1021	U.S. Patent No. 5,510,281 ("*Ghezzo*")
1022	J. A. Cooper, Jr. et al., "Status and Prospects for SiC Power MOSFETs," IEEE Transactions on Electron Devices, vol. 49, no. 4, April 2002
1023	S-H Ryu et al., "10 A, 2.4 kV Power DiMOSFETs in 4H-SiC," IEEE Electron Device Letters, vol. 23, no. 6, June 2002
1024	S-H Ryu et al., "2 kV 4H-SiC DMOSFETs for Low Loss, High Frequency Switching Applications," International Journal of High Speed Electronics and Systems, vol. 14, no. 3, 2004
1025	Plaintiff's Disclosure of Earliest Date of Invention
1026	Scheduling Order, *The Trustees of Purdue University v. STMicroelectronics, Inc. et al.*, No. 6:21-cv-00727 (W.D. Tex.), Dkt. 45 (November 22, 2021)
1027	Statistics from Docket Navigator showing active patent cases before Judge Alan Albright of the U.S. District Court for the Western Digital of Texas (as of December 6, 2021)
1028	Article entitled "District Court Trial Dates Tend to Slip After PTAB Discretionary Denials" (July 24, 2020)

CERTIFICATE UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,648, which is less than the 14,000 words allowed under 37 CFR § 42.24(a)(1)(i).

Respectfully submitted,

Dated: December 6, 2021

/Scott Bertulli/
Scott Bertulli
Reg. No. 75,886

CERTIFICATE OF SERVICE

I hereby certify that on December 6, 2021, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 7,498,633 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 7,498,633 (EX1001–EX1028)
- Power of Attorney
- Fee Authorization
- Word Count Certification Under 37 CFR § 42.24(d)

to be served via Express Mail on the following correspondent of record as listed on PAIR:

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DATED: December 6, 2021

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